RESET NOISE SUPPRESSION IN CMOS IMAGE SENSOR

USING CHARGE CONTROL TECHNIQUE

APPROVED BY SUPERVISING COMMITTEE:

_____

Youngjoong Joo, Ph.D., Chair

_____

Eugene John, Ph.D.

_____

Bao Liu, Ph.D.

Accepted: _____

Dean, Graduate School

DEDICATION

This thesis is dedicated to my husband Akshay Balasubramanian. Thank you for your unconditional love, motivation, and support.

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by

NITYA SYAMSUNDAR, B.E.

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Nitya Syamsundar, M.S.
The University of Texas at San Antonio, 2012

Supervising Professor: Youngjoong Joo, Ph.D.

In a photodiode based CMOS image sensor, reset noise plays a significant role in limiting the detection of the sensor, especially in low light conditions. In a standard active pixel sensor (APS) the reset noise (i.e. the hard reset noise) is of the order of $\frac{kT}{C}$ where k is the Boltzmann constant, T is the temperature, and C is the photodiode capacitance of the CMOS image sensor.

Several methods for reducing the reset noise have been published in the past. In this thesis, a new circuit of the CMOS image sensor with significant reduction in the reset noise using the charge control mechanism is presented. In this technique (charge control mechanism), the reset noise is reduced by precisely determining when to stop charging the capacitive sensor. The voltage across the photodiode is monitored by employing a column level comparator which is part of a feedback circuit connected to the reset transistor.

The simulation results obtained from a 4 transistor per pixel 0.5µm CMOS technology show that the reset noise can be reduced to less than $\frac{kT}{23C}$. This noise reduction is achieved with high fill factor and without adding any image lag.

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CHAPTER ONE: INTRODUCTION

Image sensors are present in single shot digital cameras, digital video cameras, embedded in cellular phones, and many more places. The primary metric used to compare digital cameras is the pixel array size of the sensor, expressed in megapixels. The higher the megapixel count, the better the imager is the common understanding. While this is true there are many more metrics with which to compare imagers that may give a better indication of performance than raw pixel counts. Further, many of these metrics may be based on the type of imaging technology - CCD (charge coupled device), and CMOS (complementary metal oxide semiconductor) [1]. This paper will explain the fundamentals of how a digital image sensor works - how photons are converted into electrical signals, and thus images. It will detail the difference between the functionality of CCD and CMOS sensors - the two chief architectures for image sensor design. It will also discuss various metrics which are commonly used in analyzing the performance of image sensors, reset noise in CMOS sensors, existing techniques used to reduce the reset noise, and finally a new circuit will be presented which results in significant reduction in the reset noise.

A digital camera takes photographs by recording images on an electronic image sensor [2]. An image sensor is an electronic device that is capable of converting an optical image into an electronic signal. It converts the photons from the visible light to an electric current (also called photocurrent) proportional to the intensity of light falling on it. The figure 1.1 [12] shows the block diagram of the basic operation of a digital camera.

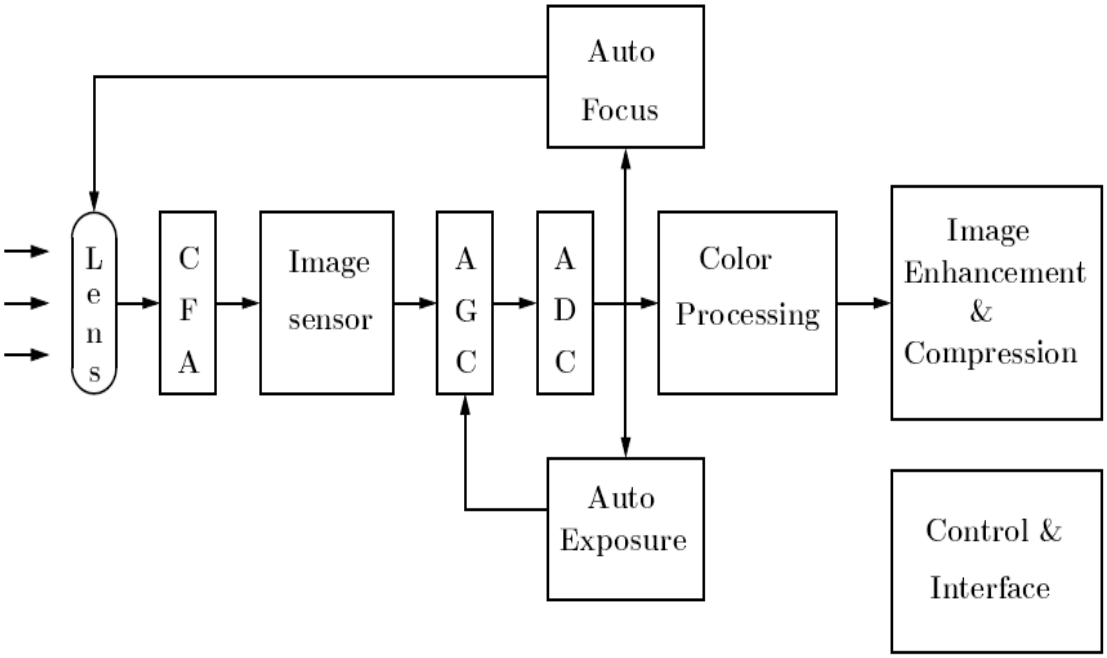

Figure 1.1: Digital camera system

The primary requirement of a camera is to capture the image of an object. To begin with light is allowed to fall on the camera lens by opening the camera shutter. The lens in the camera directs the light source to the image sensor. The image sensor is made up of an n x m array of pixels. Each pixel has a light sensitive component called the photodetector to detect the intensity of the incident light. A color filter array (CFA) is deposited on the pixels of the sensor to capture the color information from the incident light. Each pixel needs to output values corresponding to Red (R), Green (G), and Blue (B) depending on the type of color filter covering that pixel. One approach is to deposit color filters that follow a fixed pattern on the sensor. Figure 1.2 [43], shows the Bayer arrangement of red, green, and blue color filters on the pixel array. In this arrangement, each pixel in the image sensor is covered by a filter of a specific color.

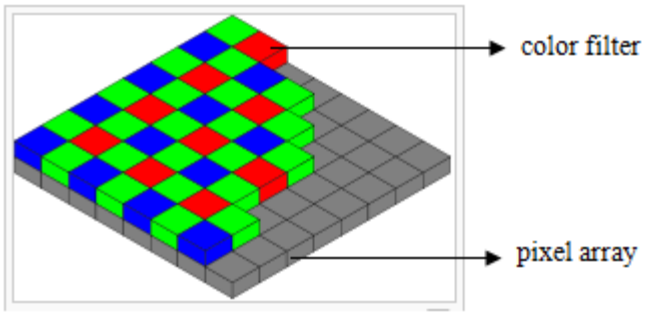

Figure 1.2: RGB Bayer arrangement of color filters on the pixel array of a sensor

The image sensor captures the optical image and converts it to an electrical signal like voltage which is proportional to the intensity of light. The most commonly used image sensors are CCD and CMOS image sensors. Pixel size ranges from 15µm x 15µm to 3µm x 3µm. The output from the image sensor is given to automatic gain control (AGC) and analog-to-digital converter (ADC) (refer figure 1.1). All these circuits including the amplifiers used for image enhancement and processing are placed outside of the pixel array. The output from the ADC is fed to the color processing circuitry that performs color interpolation to reconstruct the missing color components, color correction and balancing to improve the appearance of color. Gamma correction and color conversion is performed before feeding the signal to digital signal processing circuits for image enhancement and compression.

As mentioned before, the two most widely used image sensors are CCD and CMOS image sensors [3]. A brief overview of the advantages and disadvantages of the two types is discussed below. The CCD image sensors dominated the industry until the advent of the CMOS image sensors. Even today the CCD has a much higher signal-to-noise (SNR) ratio compared to the CMOS image sensors. The operation of CCD also ensures high quantum efficiency and low dark currents unlike the CMOS image sensors that introduce noise and non-uniformity. However with the CCD technology it is difficult and expensive to integrate the other camera functions along

with the image sensor. This is due to the difference in the technology. On the other hand, the technology used in the manufacture of the CMOS image sensors allows them to be integrated on the same chip as the processing circuitry used in the digital cameras. CMOS image sensors also consume lower power and have much higher frame rates compared to the CCD. It finds numerous applications in PC camera, web camera, games, biometrics, cell phones, and PDA. A detailed discussion of the operation of CCD and CMOS image sensors will be seen in the chapter 3 of this documentation.

Some of the metrics used to compare the performance of an image sensor are quantum efficiency (QE), sensor conversion gain, fill factor, well capacity, dynamic range, and SNR. QE is determined by the characteristics of the photodetector which converts the incident light to photocurrent [4]. QE is a measure of the optical to electrical conversion factor for a detector at a specific wavelength λ. Spectral response is the fraction of photon flux that contributes to the generation of photocurrent as a function of λ. The time for which light is allowed to fall over the sensitive portion of the sensor is called exposure time. The generated photocurrent is integrated over the exposure time into charge. This is called as the integration period or exposure period. Usually this charge is converted into voltage before it is read out of the pixel to build the image. The efficiency of the charge to voltage conversion is measured by the sensor conversion gain. The fill factor of a pixel is the ratio of the light sensitive area versus total area of a pixel [5][6]. A part of the area of an image sensor pixel is always used for transistors, electrodes, and registers which belong to the structure of the pixel of the corresponding image sensor (CCD, CMOS). Only the light sensitive part contributes to the sensitivity of the sensor.

The SNR of an image sensor is one of the most important metrics used to compare its performance. It is especially dominant under low light conditions. Image noise is an undesirable

by-product that adds spurious and extraneous information to the image. It is the random variation in brightness or color information in images. It usually originates from the electronic noise produced by the sensor and circuitry of a digital camera. The different types of noise in an image sensor with special emphasis on the reset noise will be discussed in chapter 4.

This documentation will provide the basic understanding of the design of the image sensors – CMOS and CCD. We will also discuss the performance measures and the tradeoffs involved in the sensor design along with the influence of the different types of noise. The only major disadvantage of CMOS sensors over CCD sensors is the addition of noise that reduces their SNR. Reset noise sets the fundamental detection limit on the photodiode based CMOS image sensors. We will discuss the design and operation of some of the known APS (Active Pixel Sensor) CMOS image sensors that minimize the reset noise. Finally, we will present the proposed new circuit along with its design, operation, simulation results, and noise analysis. The new circuit is implemented using the charge control technique and it reduces the reset noise by more than 23 times. We will evaluate and compare the performance of the new circuit with the existing ones based on different parameters including RNRF (reset noise reduction factor), fill factor, and speed of operation.

CHAPTER TWO: STUDY OF PHOTODETECTORS

2.1 Introduction

A Photodetector is the most important component in an image sensor. Every pixel of the sensor has a photodetector that converts the radiant power (photons/s) of the visible light incident on it into photocurrent which is proportional to its intensity [7]. The visible light is made up of photons and has its wavelength λ, ranging from 400nm to 700nm. The photon energy is given by the equation $E_{ph} = \frac{hc}{\lambda}$, where h is the Planck's constant, c = 3.8x 10^8 m/s is the speed of light, and λ is the wavelength of the incident light. Substituting the h, c, and λ values of visible light, photon energy E_{ph} of the range of 3.1 eV (corresponding to violet) to 1.77 eV (corresponding to red) is obtained. Incidentally, the forbidden energy gap in silicon to excite an electron from the valence band to conduction band is 1.124 eV. This indicates that visible light has sufficient energy to excite an electron from the valence band to the conduction band resulting in the generation of an electron hole pair. Every photon in the visible range can produce no more than one electron hole pair. The figure 2.1 [12] shows the plot of the spectral response of a silicon photodiode (type of photodetector) as a function of λ.

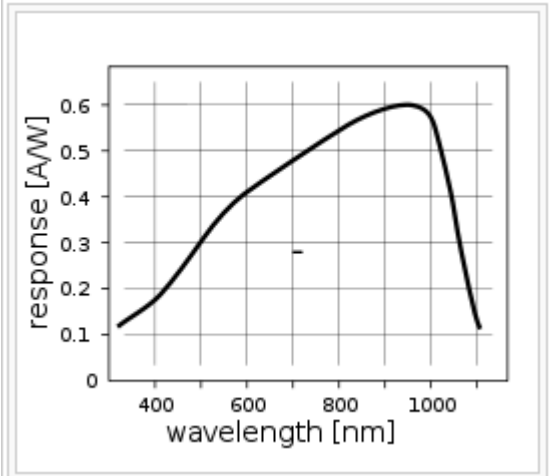

Figure 2.1: Response of a silicon photodiode vs. wavelength of the incident light

The basic operation of a photodetector is as follows: photons from the visible light are absorbed by the silicon material in the photodetector and generate electron hole pairs. Some of these carriers generated are converted into photocurrent. This photocurrent is integrated into charge and converted into voltage by direct integration before it is read out to process the image captured by the camera. The most commonly used photodetectors in image sensors are photodiodes and photogates.

2.2 Photodiodes

A photodiode is a pn junction that is reverse biased. Photodiodes are similar to regular semiconductor diodes except that they are packaged with a window or an optical fiber connection to allow light to reach the light sensitive part of the device. A photodiode is designed to operate in reverse bias. There are three types of photodiodes available: N-well/P-sub, N^+/P-sub, and P^+/N-well.

2.2.1 Basic operation of a photodiode

A photodiode is a P-N junction. When a photon of sufficient energy strikes the diode, it excites an electron, thereby creating a free electron and a positively charged hole. This mechanism is called as photoelectric effect. If the absorption of the photon occurs in the depletion region of the junction, these charge carriers are swept away by the built in field of the depletion region. The holes move towards the anode and the electrons move towards the cathode and it results in the generation of photocurrent. The photocurrent is the sum of the light current (i.e. the current generated by the generation of charge carriers when exposed to light) and the dark current (charge carriers generated in the dark without light) [8][9]. It is required to minimize the dark current to help improve the sensitivity of the photodetector. The photodiode may operate in two modes which are photovoltaic mode and photoconductive mode.

2.2.2 Photovoltaic Mode

When the photodiode is operated without the application of external bias, it is said to operate in photovoltaic mode. This method is employed in applications involving solar cells.

2.2.3 Photoconductive Mode

In the photoconductive mode, the diode is reverse biased by applying a positive voltage to the cathode. This drastically decreases the response time of the photodiode but also adds the noise. Dark current is also generated when the photodiode is operated in reverse bias due to the saturation current of the semiconductor junction.

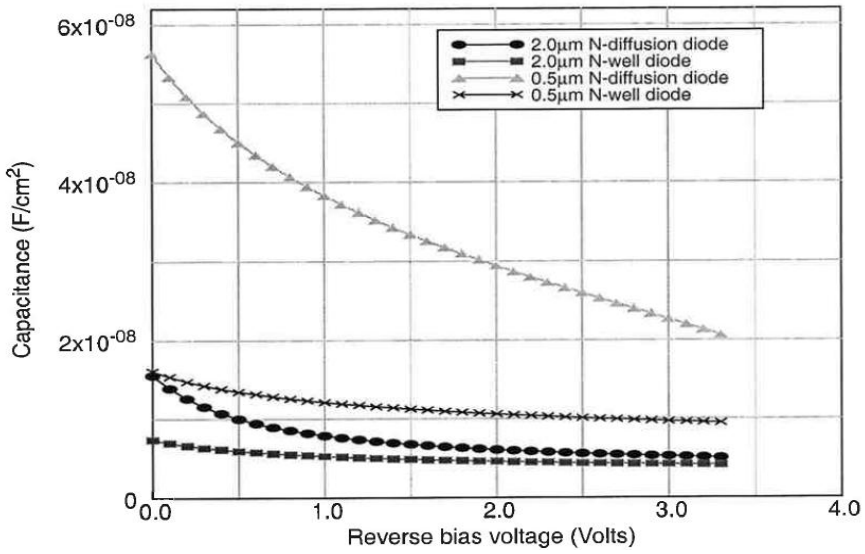

Figure 2.2: Capacitance measurement of the photodiodes

The application of reverse bias results in an increase in the width of the depletion region. This causes reduced junction capacitance thus bringing down the response time. Diode capacitance determines the conversion gain of a voltage sensing active image sensor. As the sensing capacitance gets smaller the output signal voltage becomes larger. As shown in the figure 2.2 [12] the capacitance of the N-well diodes is smaller than that of the N^+ diffusion diodes. This is due to the doping profile difference of the two P-N junctions. The lightly doped

N-well/P-sub has a wider depletion width which leads to a smaller capacitance and a larger conversion gain.

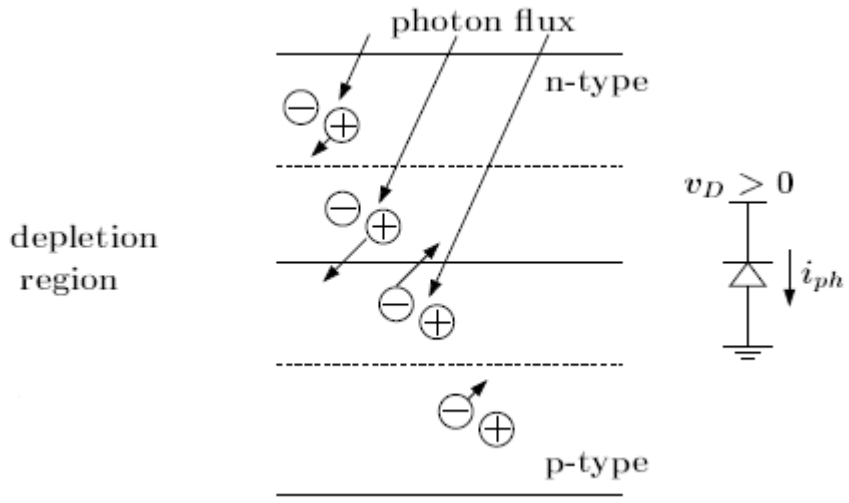

Figure 2.3: Depletion approximation

The concept of depletion approximation as shown in figure 2.3 [12] is employed in the photocurrent derivation [10]. It is an idealization of the actual charge distribution in the depletion region that originates from the fact that the majority carriers have been removed. We say this region is "depleted" of majority carriers. When using depletion approximation, we are assuming that the carrier concentration (n and p) is negligible compared to the net doping concentration (N_A and N_D) in the region. Outside this region, it is assumed that the net charge density is zero.

The photon flux at depth x of the silicon material F(x) is given by $F(x) = F_0e^{-\alpha x}$. Here F_0 is the photon flux in photons/cm^2 at depth x = 0 i.e. at the surface of the silicon material, and α is the absorption co-efficient in cm^{-1}. Also the rate of generation of electron hole pairs at depth x in the silicon material is given by:

$$G(x) = \frac{d}{dx}(F_0 - F(x)) = \alpha F_0 e^{-\alpha x} \text{ e-h pair/cm}^3\text{s} \qquad (2.1)$$

It has been proved that about 99% of violet and blue wavelengths of the visible light are absorbed by the silicon material within a depth of 0.6 µm. This is because the short wavelength

photons tend to get absorbed and generate carriers near the silicon surface. The red wavelength (which is the longest wavelength in the visible range) is absorbed at a depth of around 16.5 µm. These values match the junction depths of a CMOS process and hence allow complete absorption of the photons for the generation of photocurrent. The photodetector generates photocurrent from the electron hole pairs generated using the absorbed photon flux.

Many diodes which are designed for use specifically as a photodiode use a PIN junction rather than a P-N junction to increase the speed of response. A PIN junction has a wide, lightly doped 'near' intrinsic semiconductor region between a p-type semiconductor and an n-type semiconductor region. The p-type and n-type regions are typically heavily doped because they are used for ohmic contacts. The wide intrinsic region is in contrast to an ordinary P-N junction. The wide intrinsic region makes the PIN diode an inferior rectifier (one typical function of a diode), but it makes the PIN diode suitable for attenuators, fast switches, photodetectors, and high voltage power electronics applications.

2.3 Photogates

A photogate is another type of photodetector used for photodetection. It is a MOS capacitor. The two types of photogates in use are: NMOS transistor gate to drain and PMOS transistor gate to drain. Photogates are used in frame transfer CCD and CMOS photogate APS (Active Pixel Sensor). In CMOS technology a photogate is implemented using a MOS transistor’s gate and drain as shown in figure 2.4 [12].

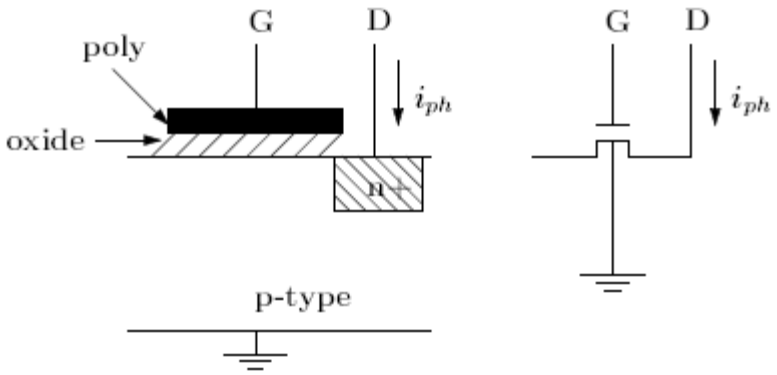

Figure 2.4: Photogate as a MOS capacitor

2.3.1 Operation of a photogate in frame transfer CCD

A photogate is a MOS capacitor exposed to light [11]. When a positive voltage (V_G), is applied to the polysilicon gate, photo generation of carriers occurs in the depletion region which is formed under the gate and in the neutral region. During the integration time, photons from the incident light pass through the polysilicon gate and generate hole-electron pairs. Holes are expelled from the depletion region to the substrate due to the developed electric field in the depletion region. On the other side, electrons are attracted by the gate and are accumulated in the silicon surface underneath the gate. The photogate is biased positively at V_{DD}, creating a potential well in the deep-depleted substrate. This is why the MOS capacitor is analogous to a bucket which can be filled with charges. The gate voltage V_G is set much greater than the threshold voltage (V_{th}) to bias the transistor into the deep depletion regime. The photocurrent i_{ph} has two components. The first component is the drift current due to the drift of holes and electrons in the depletion region, and the second component is the diffusion current due to the diffusion of photocarriers outside the depletion region. The photogate is used in direct integration mode i.e. the generated photocurrent is integrated into charge. Then the charge accumulated on

the gate is transferred to another capacitor. The CCD sensors are implemented using closely spaced MOS capacitors that behave like a dynamic charge shift register.

2.3.2 Operation of a CMOS photogate APS

The basic sequence of operations for a CMOS photogate APS are: signal integration, reset, and charge transfer [11]. During signal integration, X_i and Reset i (refer figure 2.5 [12]) are biased lower than the photogate to prevent charges from spilling over from a full well, and avoiding charge flow into adjacent pixels. Before every read out operation, the floating node D_{ij} is reset to $V_D = V_{DD} - V_{th}$ to improve noise reduction. In order to transfer the accumulated charge on the photogate to the floating node D_{ij}, the transfer gate X_i is given an intermediate voltage that is less than half the supply voltage (V_{DD}) and the gate voltage is decreased to 0V. After charge transfer the signal Word i is pulsed high and the voltage is read out of the corresponding pixel. The schematic and timing controls of the photogate APS is shown in figure 2.5 and figure 2.6 [12] respectively.

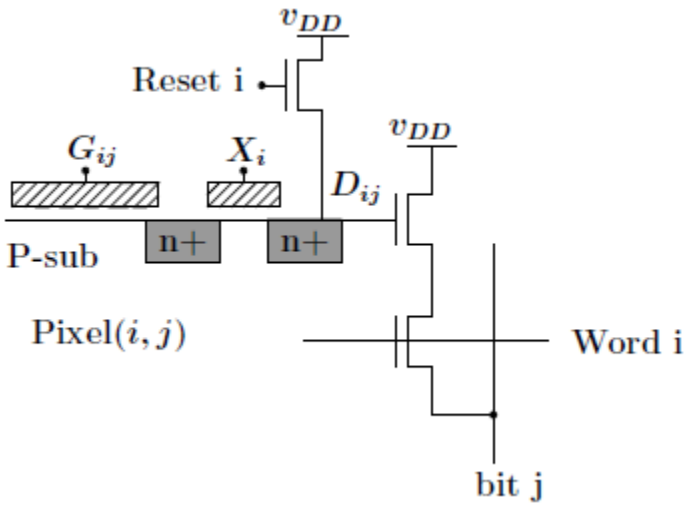

Figure 2.5: CMOS photogate active pixel sensor

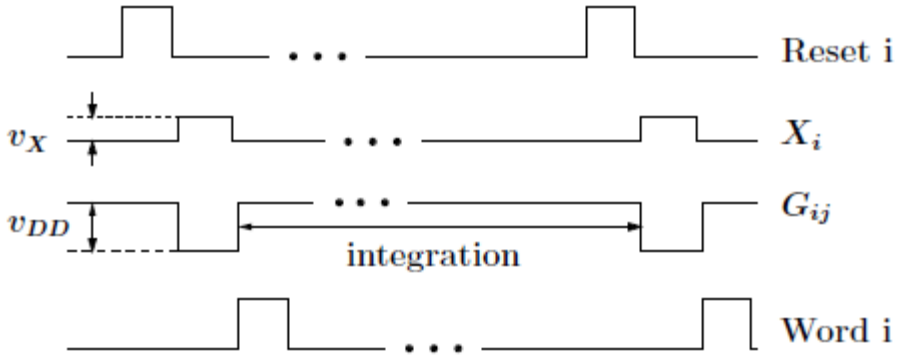

Figure 2.6: Input signal waveforms for CMOS photogate APS

Photogate achieves higher conversion gain than photodiode APS. The disadvantage with photogates is a lower spectral response for the lower wavelengths (i.e. the blue component of the visible light). This occurs because of the absorption of the blue wavelength in the polysilicon gate that has the same absorption co-efficient α, as crystalline silicon. So the bulk of the blue component from visible light (that has the smallest wavelength) is absorbed in the gate and it results in the lower response for blue. Also photogates require a larger pixel area or lower fill factor than photodiodes.

As discussed before a photodetector is the photosensitive component in every pixel of the image sensor. The operation of the two types of photodetectors: namely photodiodes and photogates were discussed in this chapter. The operation of the different types of image sensors is explained in the next chapter.

CHAPTER THREE: TYPES OF IMAGE SENSORS AND THEIR OPERATION

An image sensor is an electronic device that is capable of reacting to the light or photons incident on it. It converts the photons in the visible light to an electric current (or photocurrent) proportional to the intensity of light falling on it. The image sensor is made up of millions of pixels that essentially count the number of photons that strike the sensor. A sensor uses an array of pixels to capture the image. There are two types of image sensors –Charge Coupled Device (also known as CCD) and CMOS image sensors [12]. Both the sensors capture light and convert it to electrical signals. One major variation between the two is the difference in their read out architecture. In CCD the charge is shifted out of the pixel array and in CMOS image sensors the charge or voltage (depending on where it is passive pixel sensor or active pixel sensor) is read out of every individual pixel using row and column decoders. This read out circuitry determines the sensor conversion gain. Sensor conversion gain is the output voltage per electron collected by the photodetector. The read out speed also influences the frame rate at which the image sensor operates.

3.1 Charge Coupled Device

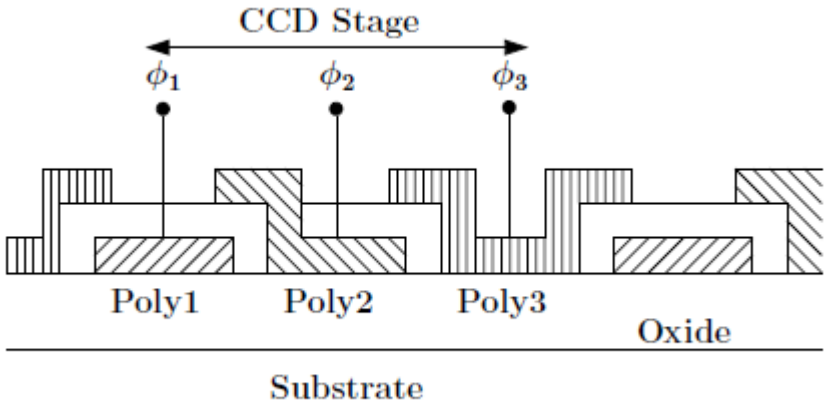

Figure 3.1: Three phase charge coupled device

Charge coupled device is a dynamic charge shift register. Photocarriers are generated in the depletion region depending on the intensity of the incident light. During integration the photocurrent is converted into charge. The charge transfer mechanism in CCD was discussed in section 2.3.1. This mechanism requires high speed clocking resulting in high power consumption. A CCD image sensor is implemented using closely spaced MOS capacitors clocked using 2, 3, or 4 phase clocks. When the clock is high, the MOS capacitor operates in deep depletion regime. The rate of charge transfer from one capacitor to the next must be high enough to prevent loss from leakage and slow enough to ensure high charge transfer efficiency. In the figure 3.1 [12], a three phase CCD is implemented using three polysilicon layers. Around 99% of the charge is transferred quickly due to the repulsive force among electrons and the remaining 1% is transferred slowly by thermal diffusion and fringing field. It is the last 1% that takes up the bulk of the transfer time which is given by:

$$\eta = (1 - 0.01e^{\frac{-t}{p\tau}})^p \tag{3.1}$$

$$\tau = \frac{4L^2}{\pi^2 D_n} \tag{3.2}$$

Here t is the CCD stage transfer time, p is the number of CCD phases used, L is the centre to centre distance of adjacent capacitors as shown in the figure 3.2 [12], and D_n is the diffusion constant at the surface.

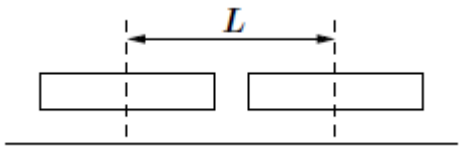

Figure 3.2: Centre to centre distance of adjacent capacitors in a CCD array

High fill factor is one of the major advantages of the CCD image sensors. The fill factor of a pixel is the ratio of the light sensitive area versus total area of a pixel. Higher the fill factor higher the sensitivity of the image sensor. The readout speed in CCD is limited by the size of the array and the charge transfer efficiency. CCD does not introduce any noise during the shifting and has low dark currents. However it has a limited frame rate especially for large sensors. This stems from the large requirement for speed while maintaining the acceptable levels of charge transfer efficiency. Transfer time can be minimized by increasing the fringing field. This is achieved by increasing the gate voltage difference during transfer, reducing the spacing between the capacitors, overlapping the poly gates, and by using a low substrate doping. Two of the most commonly known types of CCD are frame transfer CCD and interline transfer CCD [13].

3.1.1 Frame transfer CCD

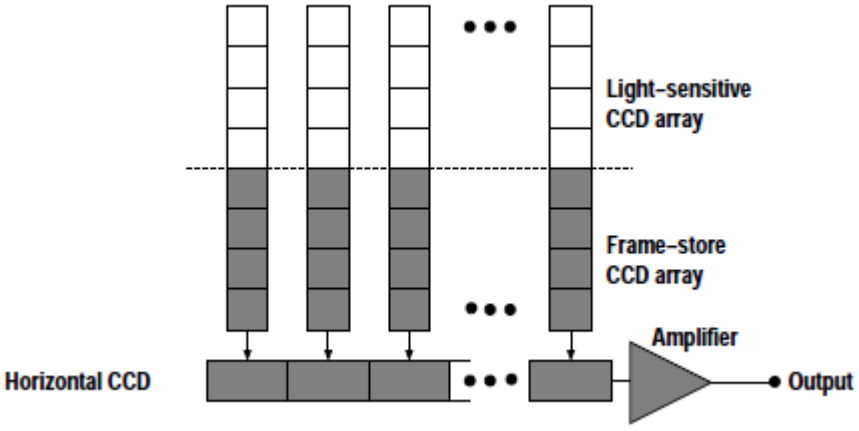

Figure 3.3: Frame transfer CCD image sensor

In the frame transfer CCD, the top portion of the pixel array is used for photodetection [14]. This half is sensitive to light and consists of photogates. The bottom half of the array is optically shielded and is used as a frame store as shown in figure 3.3 [12]. So for example, a 640x480 pixel frame transfer sensor has a 640x480 active pixel array on the top and another 640x480 storage pixel array at the bottom. The storage pixels are masked (covered) so that no

photons can hit them. This sensor captures a full frame in a single shutter (integration) period. The image capture process for a frame transfer sensor begins with the integration period, where the active pixels collect electrons that are converted from the incident photons. At the end of the integration period the 480 lines (using the example above) of active pixels (640 pixels per line) are clocked down line by line (as fast as possible) until all 640x480 pixel charges are stored in the 640x480 storage pixel array (i.e. the bottom half of the CCD array). The time it takes to clock all 480 lines from the active pixel area to the storage pixel area is called the readout time. When the readout operation is completed, the active pixels are reset and the next integration period begins, while the pixel charges in the storage area are clocked out line by line to the shift register. From the shift register they are in turn clocked out the back of the camera via amplification and conditioning circuitry. The output amplifier converts the charge into voltage and determines the sensor conversion gain.

3.1.2 Interline transfer CCD

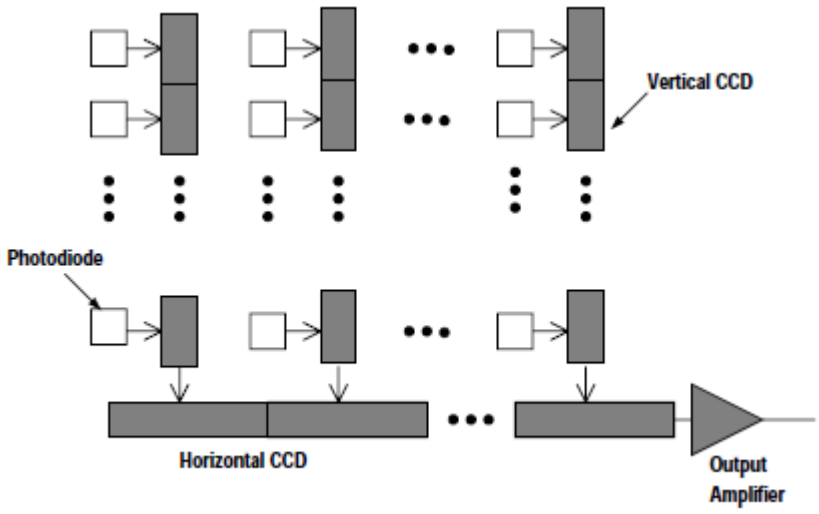

Figure 3.4: Interline transfer CCD image sensor

In an interline transfer CCD sensor, every pixel have a charge storage area next to it as shown in figure 3.4 [12] [14]. The charge storage area of each pixel is masked so that photons cannot hit it. The pixel storage areas form a vertical column to the bottom of the sensor. This vertical column is used to transport the pixel charges down and out the bottom of the sensor. The light sensitive pixel area (active area) is electrically separated from the storage pixel area and so the active pixel area can act independently of the storage area. At the end of the integration period the charge in every active pixel is shifted to its adjacent pixel storage area. At this point, the active pixel area is reset and the next integration period starts immediately while the charges in the storage pixels are clocked down to the bottom of the sensor. This happens with all pixels on a line simultaneously so that pixel charges from all the lines are clocked down together.

When a pixel charge reaches the bottom of the sensor it is clocked down once more to a shift register. The pixel charges in the shift register at any one point in time represent the pixels acquired on a row of the sensor during the earlier integration period. Once the pixel charges are in the shift register, they are clocked out at a rapid rate before the next row of pixel charges is clocked into the shift register. From the shift register, the pixel charges are fed to amplifiers which convert the charge into voltage. The voltage is then conditioned further, digitized in the case of digital cameras and then fed out the back of the camera.

Table 3.1: Comparison of frame transfer CCD with interline transfer CCD

Parameter	Frame transfer CCD	Interline transfer CCD
Photodetection with	Photogates	Photodiodes
Fill factor	100%	Lesser
Sensor area	Larger	Smaller
Frame rate	Slower	faster – around 25 frames/s

Tables 3.1, compares the performance of frame transfer CCD and interline transfer CCD. It is observed that there is a tradeoff between speed and sensitivity of the sensor. CCD charge transfer efficiency $\eta <= 1$, is the fraction of the signal charge transferred from one CCD stage to the next. η must be as close to 1 as possible for efficient charge transfer to output. The significance of high charge efficiency for a CCD image sensor is indicated by the worst case fraction of charge transferred to output for different values of charge efficiency in Table 3.2 [12].

Table 3.2: Relation between η and fraction of output charge

Charge Transfer Efficiency, η	Worst case fraction of charge transferred to output
0.999	0.1289
0.9999	0.8148
0.99999	0.9797

To summarize, CCD image sensors have high quality in terms of high quantum efficiency, low dark currents, very low noise, and very low fixed pattern noise (FPN) [15][16]. Also no noise or FPN is introduced during shifting. However it cannot be integrated with other analog or digital circuitry. It is very difficult to realize a window of interest i.e. it is non-programmable, has high power consumption as the CCD array is constantly switching. It demands high clock frequency and high voltage for efficient operation, and gives only a limited frame rate in comparison to the CMOS image sensors [17].

3.2 CMOS Image Sensors

In a CMOS image sensor, each pixel comprises of a photodiode and some extra circuitry to convert the light energy to charge or voltage (depending on the type of sensor). The pixel level operation of the CMOS sensor is as follows: first the photodiode in the pixel is reset to a reverse

bias voltage. Then the photodiode is exposed to light and depending on the intensity of light, the diode current discharges the diode capacitance. At the end of the integration period, the accumulated negative charge or the output voltage is read out of the pixel. Thus knowing the initial reset voltage and the voltage after integration gives an accurate measure of the intensity of the incident light. CMOS image sensors are classified into two types: passive pixel sensor (PPS) and active pixel sensor (APS).

3.2.1 CMOS Passive Pixel Sensor

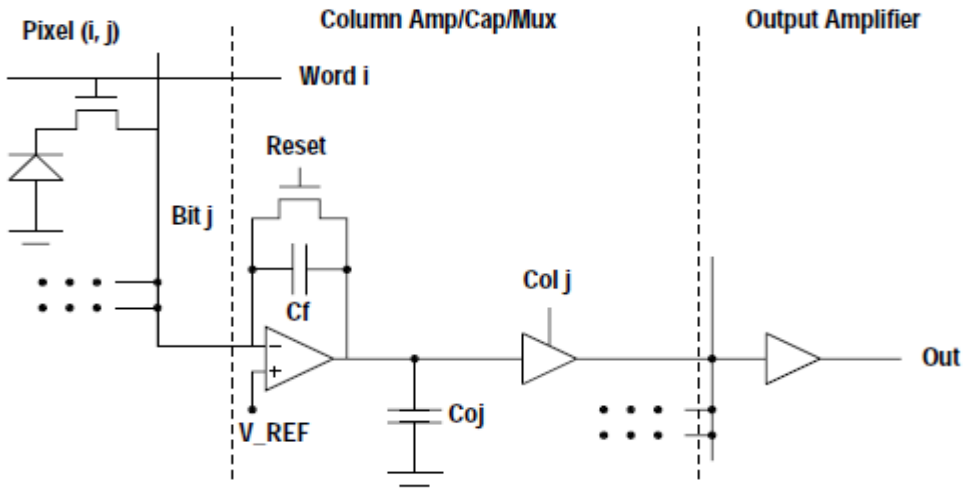

Figure 3.5: CMOS passive pixel sensor

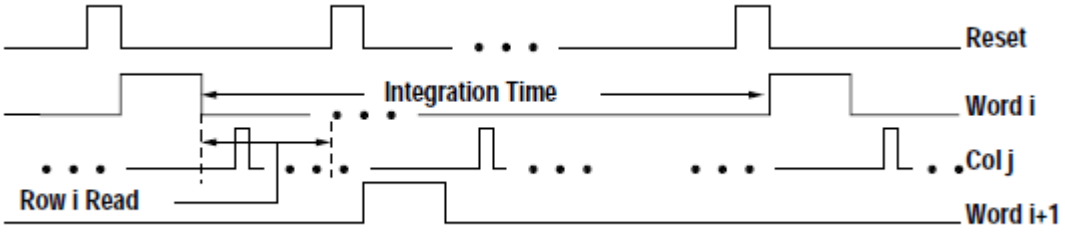

Figure 3.6: Control signal waveforms for CMOS PPS

A CMOS PPS pixel has a photodiode and a transistor. The schematic is shown in figure 3.5 [12] while its timing is in figure 3.6 [12]. The PPS pixel operation has three steps – reset,

integration, and readout. During reset a reverse bias voltage V_{REF} is applied. Then the sensor is exposed to light and the photodiode discharges depending on the intensity of light falling on it. During integration the generated photocurrent is converted to charge. The charge is read out of the pixel using column charge amplifier. Reading is destructive in CMOS PPS imagers. In PPS readout is performed row wise. The row of pixels is selected one after the other using a row decoder. The charge to voltage conversion occurs at column level using column and chip amplifiers that are simple source followers. The column readout time is controlled by sizing the column and chip follower amplifiers. Row readout is done in two steps – first the row signal is transferred to the column capacitors, then the column decoder/multiplexer is used to serially read out the pixel values. So the row readout time is a dominant factor in PPS. If Q is the charge accumulated on the photodiode at the end of the integration period, then the output voltage is:

$$V_o = V_{REF} + \frac{Q}{C_f} \tag{3.3}$$

Here the sensor conversion gain is $\frac{Q}{C_f}$. Output voltage takes a minimum value when Q = 0 i.e. when no light falls on the sensor or in dim light, and a maximum value when the voltage on the diode reaches ground i.e.in bright light when the photodiode discharges from V_{REF} to ground:

$$V_{omin} = V_{REF} \tag{3.4}$$

$$V_{omax} = V_{REF} + \frac{C_D}{C_f} V_{REF} \tag{3.5}$$

Here C_D is the photodiode capacitance. PPS is slow and has a low signal to noise ratio (SNR).

3.2.2 CMOS Active Pixel Sensor

An active-pixel sensor (APS) is an image sensor containing an array of pixel sensors where each pixel contains a photodetector and an active amplifier [18][19][20]. CMOS APS has

3 or 4 transistor per pixel in addition to the photodiode. The charge to voltage conversion occurs within each pixel unlike PPS where the conversion occurs at column level.

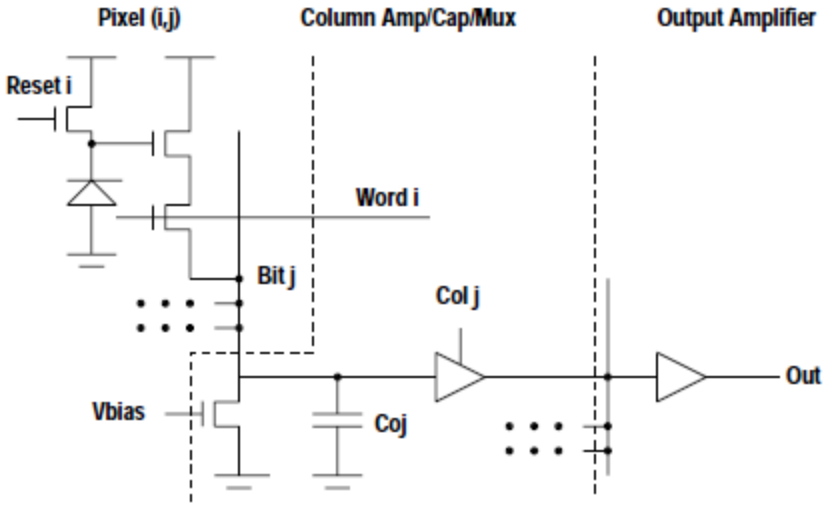

Figure 3.7: CMOS active pixel sensor

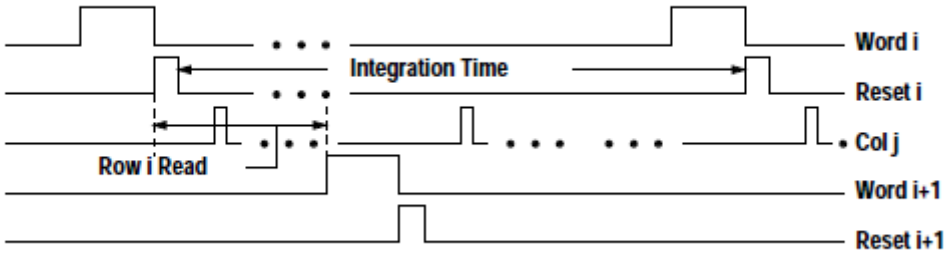

Figure 3.8: Control signal waveforms for CMOS APS

The term active pixel sensor is also used to refer to the individual pixel sensor itself, as opposed to the image sensor [21][22]. Figure 3.7 [12] is the schematic of a 3T APS consisting of a photodiode, reset transistor, source follower, selection transistor, and the column level circuitry. The control signals for APS are shown in figure 3.8 [12]. The reset transistor acts like a switch to reset the photodiode. When reset transistor is ON using the signal Reset i, the photodiode corresponding to pixel (i, j) is connected to the power supply and the diode is reset to

a reverse bias voltage equal to the supply voltage. At the end of the reset period the reset transistor is abruptly turned OFF. Now the photodiode is cut OFF from the power supply and is exposed to light and the diode capacitance discharges from supply voltage to a value depending on the intensity of the light falling on it. Direct integration is employed and the output voltage is read out of the pixel. Reading is not destructive as the output voltage of the photodiode is buffered using pixel level follower amplifier. Thus knowing the initial reset voltage and the pixel output voltage after integration, information about the incident light is obtained. Each row of pixels has separate reset. Reset is employed after every read out operation. The photodiode reset voltage is:

$$V_D = V_{DD} - V_{th} \tag{3.6}$$

Here V_{DD} is the voltage supplied to the drain of the reset transistor and V_{th} is the reset transistor threshold voltage. Figure 3.9 [12] is the pixel level schematic of APS.

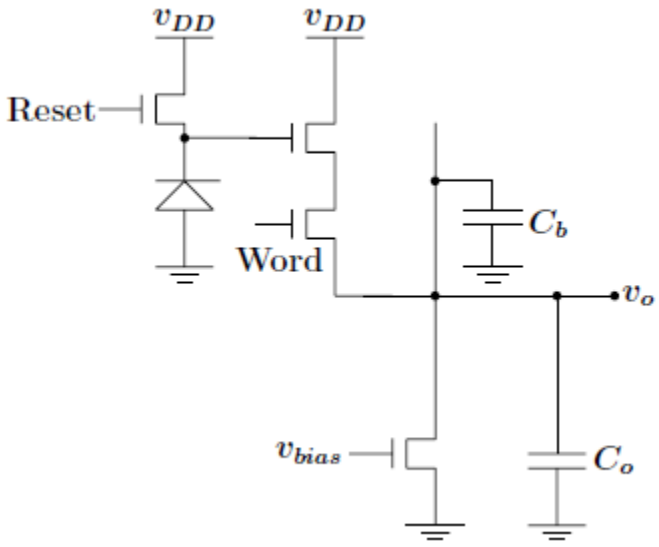

Figure 3.9: 3T active pixel sensor at pixel level without column level circuitry

If Q is the charge accumulated on the photodiode at the end of the integration, the pixel output voltage is given by:

$$V_o = V_D - \frac{Q}{C_D} - V_{GSF} \quad (3.7)$$

Here C_D is the photodiode capacitance and V_{GSF} is the gate to source voltage of the source follower transistor. The sensor conversion gain is given by $\frac{Q}{C_D}$ uV/electron. This expression for output voltage is obtained by ignoring the voltage drop across the access transistor controlled by the signal Word. When Word goes high the output voltage is read out from the corresponding pixel in the row. Substituting for V_D we get:

$$V_o = V_{DD} - V_{th} - \frac{Q}{C_D} - V_{GSF} \quad (3.8)$$

The readout speed of the APS is equal to the sum of the time to transfer charge from the row to column capacitors plus the time to read out the pixel values from column multiplexer. The former is called the row readout time and the later is called the column readout time. In APS the column readout time is the dominant factor. A comparison between PPS and APS is in Table 3.3.

Table 3.3: Comparison of CMOS PPS and APS

Parameter	CMOS PPS	CMOS APS
# of Transistors per pixel	1	3-4
Fill factor	Higher	Lower
Speed	Slow	Fast
Signal to noise ratio (SNR)	Low	Higher

In the forthcoming discussions we will be focusing on CMOS image sensors.

CHAPTER FOUR: NOISE IN CMOS IMAGE SENSORS

Noise is an unwanted disturbance that obscures or interferes with the desired signal. In addition to the dark current generated by the photodiode when operated in photoconductive mode, there are other sources of noise in an image sensor that limits the sensitivity and dynamic range of the device. Dynamic range of a signal refers to the ratio of the largest possible signal to the smallest signal it can generate. The largest possible signal is directly proportional to the well capacity of the pixel and the lowest signal is the noise level when the sensor is not exposed to any light [23]. This is referred to as noise floor. Full well capacity refers to the amount of charge an individual pixel can hold before it saturates.

4.1 Temporal Noise

Temporal noise is the variation in the pixel output values under uniform illumination due to device noise, e.g. thermal noise, shot noise, substrate noise, and supply voltage fluctuations [24][25][26]. This temporal noise increases with signal however the rate at which the signal increases is much higher than the rate at which noise increases which implies that these noise factors are more pronounced at low signal values i.e. under low illumination. The temporal noise under low light conditions limits the dynamic range of the sensor. In a CMOS APS, several additional sources contribute to temporal noise including the noise due to the pixel reset, source follower, and access transistors. The analysis of noise is further complicated by the nonlinearity of the APS charge to voltage characteristics, which is becoming more pronounced as CMOS technology scales down, and the fact that the reset transistor operates below threshold or in sub-threshold region for most of the reset time. The non linearity in APS is because the charge to voltage conversion is done using the photodiode capacitance (non-linear component) unlike PPS

that uses the column charge amplifier (which can be made linear). The most significant forms of temporal noise in CMOS image sensor is thermal noise, shot noise, and flicker noise.

4.1.1 Thermal Noise

The reset noise of capacitive sensors is often a limiting noise source in image sensors. The thermal noise is generated by the thermally induced motion of electrons in resistive regions like a MOS transistor that is operated in its linear region. This occurs when the transistor channel is in strong inversion. In a CMOS APS, this noise occurs at the end of the reset operation when the reset transistor (acting as a switch) is abruptly turned OFF. The noise is not caused by the photodiode capacitor itself, but by the thermodynamic equilibrium of the amount of charge on the capacitor at the end of reset. Once the capacitor is disconnected from a conducting circuit, the thermodynamic fluctuation is frozen at a random value with variance given by:

$$\sigma^2 = \frac{kT}{C} \tag{4.1}$$

Here k is the Boltzmann's constant, T is the temperature, and C is the photodiode capacitance of the image sensor. The above expression will be derived later in this chapter.

4.1.2 Shot Noise

The shot noise is generated by the fluctuations in static or dc current flow through the depletion region like in a pn junction diode [9]. Shot noise is a type of electronic noise which originates from the discrete nature of electric charge. The term also applies to photon counting in optical devices, where shot noise is associated with the particle nature of light. Shot noise is dominant when the finite number of particles that carry energy (such as electrons in an electronic circuit or photons in an optical device) are sufficiently small such that the uncertainties due to the Poisson distribution, which describe the occurrence of independent random events are of significance. Each photon induces a free electron and every electron contributes to the signal

current. Hence fluctuations in the number of photons create a fluctuation in the signal current and contribute to shot noise.

Shot noise has zero mean, very flat, and wide bandwidth power spectral density. It is modeled as a white Gaussian noise (WGN) current source in parallel with the dc source i as shown in figure 4.1 [12].

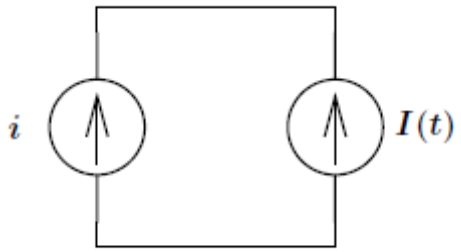

Figure 4.1: Shot noise modeled as a WGN current source in parallel with a dc source

Its power spectral density over all frequencies is given by:

$$S_I(f) = qi\ A^2/Hz \qquad (4.2)$$

Here q is the electron charge in Coulomb.

4.1.3 Flicker Noise

The flicker noise is caused by the static current flow in both the resistive and depletion regions that is caused by the random capture and release of carriers due to the crystal defects. Flicker noise has a zero mean and a power spectral density (PSD) that decreases drastically with increase in frequency. This is because some of the time constants associated with the release and capture of carriers are relatively long. The PSD is give by:

$$S_I(f) \alpha \frac{i^c}{|f|^n} \qquad (4.3)$$

Here ½ ≤ c ≤ 2 and for n = 1 flicker noise is also called $\frac{1}{f}$ noise. $\frac{1}{f}$ noise is very significant at low frequencies.

The most dominant source of noise in a photodiode is shot noise and flicker noise. In a MOS transistor the most dominant noise source is dependent upon the operating point of the transistor [27] [28]. When the transistor is used as a switch its channel is in strong inversion and thermal noise is the dominant source of noise. When in sub threshold region the shot noise is the most dominant noise source. Flicker noise is also present in the transistor due to the presence of slow traps at the gate oxide.

4.2 Photodiode Operation in a CMOS Image Sensor

In a CMOS image sensor, the photo current and dark current generated are directly integrated over the diode capacitance. Firstly, the photodiode is reset to a reverse bias voltage V_D, which is also the reset voltage. After a few microseconds of reset operation, the reset transistor is abruptly turned OFF. The reset operation is followed by integration period.

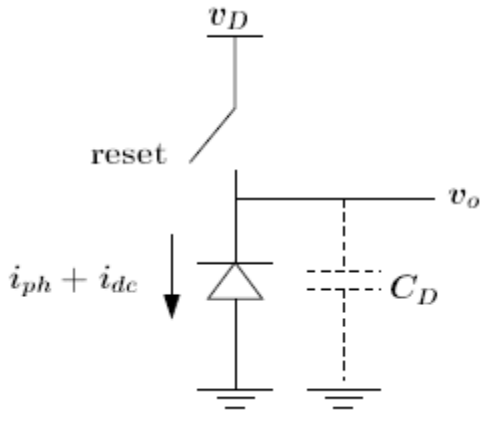

Figure 4.2: Direct integration of photocurrent over diode capacitance

During integration period the shutter is opened to allow light to reach the sensitive part of the device. When the photodiode is exposed to light, depending on the intensity of light, the

diode current discharges the diode capacitance C_D (refer figure 4.2 [12]) for t_{int} seconds which is the integration time or the exposure time.

At the end of the integration time the accumulated negative charge or the output voltage is read out. Thus knowing the initial reset voltage and the voltage after integration gives an accurate measure of the intensity of the incident light. If the previous exposure was bright light, the diode capacitance is fully discharged, however if the previous exposure was low light, then there is some residue voltage in the diode capacitance which might influence the next exposure. This is called the image lag [29]. Thus the reset operation performed must be accurate to minimize image lag situations. The concept of image lag is explained again under hard reset and soft reset. The thermal noise from the reset transistor, shot noise from the photodiode, and a negligible amount of flicker noise results in ambiguity about the exact reset voltage. This reset noise cannot be completely eliminated due to the inherent characteristics of the transistors, diodes, and transistors [27] [28]. In addition to the reset noise there is also the read noise contributed by the read out circuitry, fixed pattern noise, noise from the power supply fluctuations, and other external and environmental factors that offsets the accuracy of the photodiode operation.

4.3 Reset Techniques

Noise can originate in: voltage conversion, the source follower amplifier, and the readout amplification chain, including the analog-to-digital converter (ADC) quantizing noise. The read noise for a system sets the lower limit for a resolvable signal. Therefore, a low read noise is advantageous for lowlight applications. The major source of noise in a CMOS APS imager is the reset noise that is induced when the sense node (photodiode) capacitor is reset. Hence the dominant noise source in a 3T APS imager is the $\frac{kT}{C}$ noise introduced during the reset

operation. The pixel can be reset using hard reset, soft reset, or active reset technique. In the following section the advantages and disadvantages of each technique is discussed.

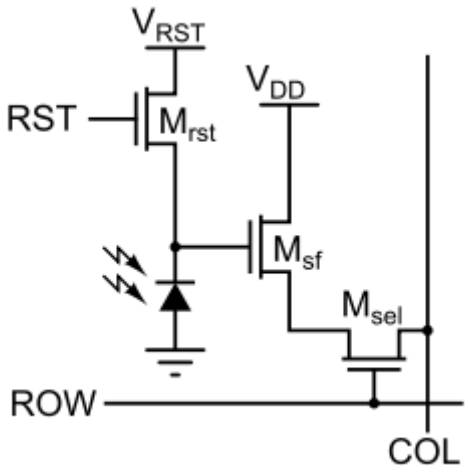

Figure 4.3: 3T CMOS APS

4.3.1 Hard Reset

Hard reset refers to the condition when the reset transistor M_{rst}, (refer figure 4.3 [1]) is in strong inversion during the reset operation. When M_{rst} is turned ON and is operating in the linear region, the photodiode gets charged to V_{RST}. Soon it reaches a state of thermal equilibrium with V_{RST}. At the end of the reset operation, the reset transistor is turned OFF abruptly resulting in an uncertainty in the actual charge on the photodiode capacitor due to the Brownian motion of electrons. This uncertainty is referred to as the reset noise and its noise variance is given by $\frac{kT}{C}$ which will be derived in section 4.3.4 (refer equation 4.9) [30].

4.3.2 Soft reset

During soft reset, the reset transistor M_{rst}, (refer figure 4.3 [1]) operates in the sub-threshold region [31]. This is achieved when RST and V_{RST} are both of the same potential. As a result, the photodiode and V_{RST} will never reach thermal equilibrium in soft reset. There is

always a difference of voltage less than or equal to the threshold voltage V_{th} between them. As a result, the Brownian motion or the random motion of electrons is unidirectional during soft reset as opposed to the bi-directional motion of electrons in hard reset. In soft reset, the photodiode potential is always less than the potential at the drain of M_{rst}. So the carriers are emitted from the photodiode to the reset drain under the effective barrier of the reset gate. Hence the noise variance is reduced by a factor 2. Hence the reset noise due to soft reset is given by $\frac{kT}{2C}$.

However soft reset technique results in an image lag. If the previous exposure to light is dim, the photodiode capacitance will not discharge completely. It will still have some residue charge on it during the current reset operation. This results in an image lag.

To overcome this problem, hard reset is done first followed by soft reset. This way the noise variance is reduced by half (due to soft reset) and the image lag is eliminated (due to hard reset). The reset transistor M_{rst}, is first operated in linear region (to perform hard reset) and then operated in sub threshold region (to perform soft reset). By combining the two techniques we retain the advantage from both the methods.

4.3.3 Active Reset

Active reset is a technique that combines the hard reset and soft reset mechanisms and employs feedback mechanisms to reduce the reset noise [32][33][34]. First a hard reset is done to eliminate the image lag. Next a soft reset is done to reduce the noise variance by a factor of 2. Here soft reset is preceded by hard reset so there is no additional lag introduced by soft reset. Active reset achieves much lower noise levels by monitoring the pixel voltage using feedback techniques. The tradeoff is a complicated reset scheme, a larger pixel, or extra column level circuitry. Some of the active reset techniques are discussed in the next chapter. In each method, a feedback is employed to monitor the voltage across the capacitive sensor.

4.3.4 Derivation of reset noise

During the reset operation the pixel in a CMOS image sensor can be modeled as a RC circuit (as shown in figure 4.4 [9]), where the reset transistor operating as a switch has a resistance R and C is the photodiode capacitance.

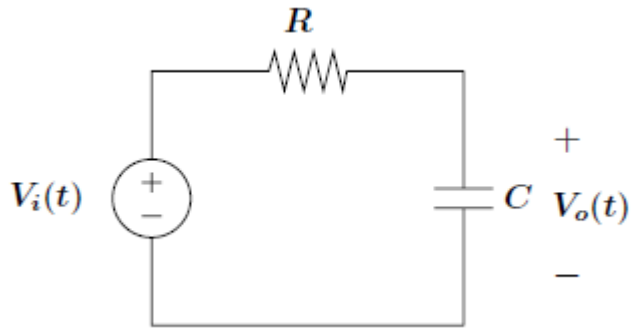

Figure 4.4: RC circuit

Here $V_i(t)$ is the thermal noise contributed by the resistor R. The thermal noise is a white Gaussian noise process with power spectral density as $S_{Vi}(f) = 2kTR$, where k is the Boltzmann's constant, T is the temperature, and R is the resistance. The transfer function is given as:

$$| H(f) |^2 = \frac{1}{1+(2\pi fRC)^2} \tag{4.4}$$

The output voltage power spectral density is given by:

$$S_{Vo}(f) = \frac{2kTR}{1+(2\pi fRC)^2} \tag{4.5}$$

And the average output noise power is given by:

$$V_o^2(t) = \int_{-\infty}^{+\infty} S_{Vo}(f)\, df \tag{4.6}$$

$$= \int_{-\infty}^{+\infty} \frac{2kTR}{1+(2\pi fRC)^2}\, df \tag{4.7}$$

$$= \frac{2kTR}{2\pi RC} \arctan(x) \Big|_{-\infty}^{+\infty} \tag{4.8}$$

$$= \frac{kT}{C} \tag{4.9}$$

The reset transistor that is operating in the linear region along with the photodiode capacitance can be modeled as an RC circuit and the above derivation applies to the thermal noise power from the reset transistor. The thermal noise and the shot noise are intrinsic characteristics of all resistors, diodes, and transistors. Even though the thermal noise originates from the random motion of thermally induced motion of electrons across a resistive region there is no R term in the expression of variance derived above. Thermal noise in an RC circuit has a simple expression as R drops out of the final equation. This is because higher R contributes to more filtering as well as to more noise. The noise bandwidth of the RC circuit is $\frac{1}{4RC}$, and hence the two resistance terms cancel each other out.

Noise in image sensors is also contributed by the photocurrent and dark current from the photodetector, the MOS transistors used in readout and amplification, substrate and supply voltage fluctuations. In a CCD sensor, a single output amplifier is used and noise analysis is quite simple. In CMOS sensors, the noise is contributed by the photodetector (during integration), source follower amplifier, access transistor (during readout), and multiple levels of column amplifiers. This makes the noise analysis in CMOS sensors more complex than CCD sensors.

In this paper we are primarily interested in minimizing the reset noise in capacitive sensors. As discussed in the previous section, the reset noise does not originate from the reset transistor or the capacitance of the photodiode. It comes from the thermodynamic equilibrium of

the amount of charge on the capacitor at the point when the reset transistor is turned OFF. This is the uncertainty in the system at thermal equilibrium which is $\frac{kT}{2}$ per degree of freedom.

The reset noise is not really noise in the physical sense. It is the ambiguity in the exact voltage to which the photodiode is reset. It is important to know the precise measurement of the reset voltage because the sensitivity of the sensor depends upon it. The reset operation is followed by the integration period. During integration, photodiode discharges depending on the intensity of light falling on it. If there is an ambiguity in the initial reset voltage the sensitivity of the image sensor is reduced especially in low light applications [20].

Thus the aim is to minimize the reset noise to improve the sensitivity of the sensor. Several ideas have been published so far in this context. Some of the papers have used the concept of feedback to minimize reset noise. We will discuss some of these ideas in detail in the next chapter before proceeding to the new circuit idea that is proposed in this paper. We will compare the results from the existing circuits and show through simulation results that this new idea proposed reduces the reset noise to a significant level while meeting the other requirements such as low reset period, fill factor, and voltage swing.

CHAPTER FIVE: STUDY OF THE EXISTING RESET NOISE REDUCTION MECHANISMS

Reset noise sets the fundamental detection limit on photodiode based CMOS image sensors. In the previous chapter the reset noise in standard active pixel sensor was studied to be of the order of $\frac{kT}{C}$ where C is the photodiode capacitance of the pixel. Some of the existing approaches to reduce the reset noise will be discussed in this chapter. The discussion for each approach will comprise of the circuit design, operation, and noise reduction analysis.

Many of the existing techniques use the concept of feedback to minimize the noise resulting from the ambiguity in the reset voltage due to the Brownian motion of electrons. In the feedback mechanisms, the photodiode voltage is compared to a known reference value. Once the photodiode reaches this value the reset operation is stopped, bringing the reset voltage to a known value. We will discuss the operation of the following techniques: correlated double sampling (CDS), bandwidth control, capacitive control, and charge control technique.

5.1 Correlated double sampling

CDS uses a column level differential readout [35][36][37][38]. Two samples of voltage are taken across the photodiode, one when the pixel is in reset state and one after integration period. These values are readout differentially to drastically minimize the $\frac{kT}{C}$ noise and the fixed pattern noise. This method is used to remove the reset noise when measuring the sensor outputs. The output of the sensor is measured twice: once in a known condition and once in an unknown condition. The value measured from the known condition is then subtracted from the unknown condition to generate a value with a known relation to the pixel output voltage.

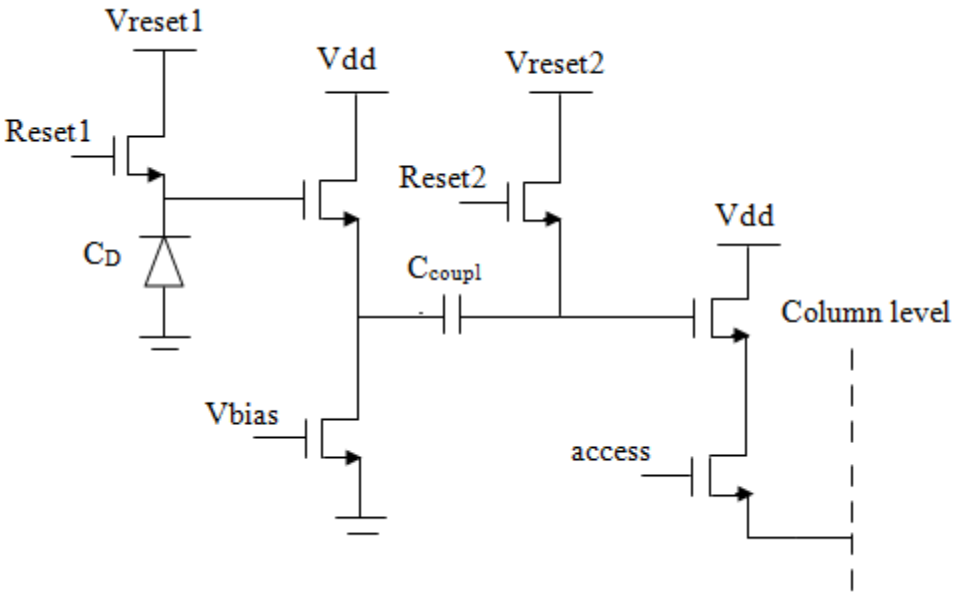

Figure 5.1: Schematic of InPixelCDS architecture

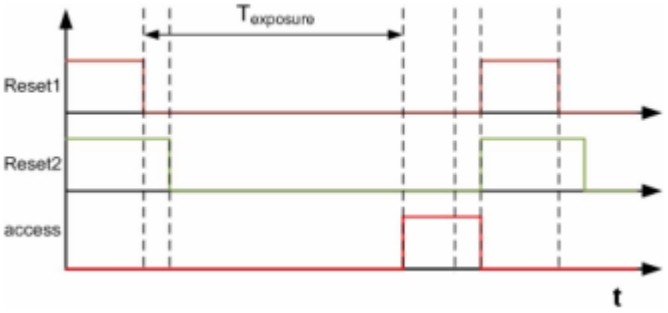

Figure 5.2: Timing waveforms for CDS

The basic operation of CDS: the signal Reset1 (refer figure 5.1 [35] and figure 5.2 [35]) goes high and the coupling capacitor C_{coupl}, between the two source followers is also reset. After the signal Reset2 goes low, the reset sample from the photodiode after amplification from the first source follower is stored on one end of C_{coupl}. At the end of the integration period, the voltage across the photodiode (it retains the reset sample) and the integrated signal is read out through the coupling capacitor. As they are stored on opposite sides of the capacitor $C_{coupl,}$ the reset noise is cancelled.

However the reset noise generated when C_{coupl} was reset still persists. In addition to the in pixel correlated double sampling it is also required to perform double sampling to the column level capacitors to remove any pixel to pixel source follower mismatches. For efficient performance of this technique it is important to size the C_{coupl} much larger than the photodiode capacitance. But this causes a reduction in the fill factor due to the use of the large sized in- pixel capacitor. Also the use of additional circuitry gives rise to other noise factors due to mismatches in transistors and high leakage current from the first source follower.

5.2 Bandwidth Control Method

In the bandwidth control method the reset noise is controlled using a feedback loop which attenuates the thermal noise of the reset transistor [39][40]. The basic mechanism is to reduce the noise bandwidth of the reset transistor less than the bandwidth of the feedback loop, in order to reduce the noise stored on the capacitive sensor below $\frac{kT}{C}$. First a hard reset is performed on the capacitive sensor. Then an error amplifier in a feedback loop is connected via a time varying resistor to the sense node. The last step is to increase the bandwidth of the time varying resistor until the bandwidth of the error amplifier is much larger than the noise bandwidth of the resistor. The time varying resistor is implemented using the reset transistor M1, (refer figure 5.3) operated in the linear region. The reset signal given to the gate of M1 is initially raised from ground to a voltage just below $V_{dd.}$ Then the voltage is decreased using a linear ramp to about $\frac{V_{dd}}{2}$ causing M1 to slowly turn OFF. By varying the gate voltage of M1 (which is operating in linear region) using the ramp signal, its resistance is varied as a function of time. The noise bandwidth of this time varying resistor (M1) is equal to $\frac{1}{4r(t)(c_{se}+c_f)}$. Also the time varying resistance r(t) must

tend to ∞ as t tends to ∞ in order to attenuate the thermal noise from M1. Using the ramp signal the resistance of M1 is increased thereby decreasing its noise bandwidth. This condition is achieved by disconnecting M1 at the end of the reset cycle. When M1 is turned OFF, its resistance tends to ∞ while its bandwidth tends to 0. The schematic for the bandwidth control method is shown in figure 5.3 [39] and its timing is shown in figure 5.4 [39].

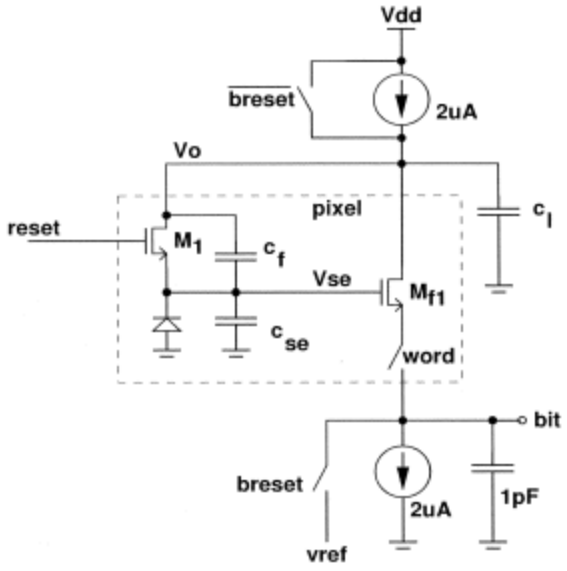

Figure 5.3: Schematic diagram for the bandwidth control method

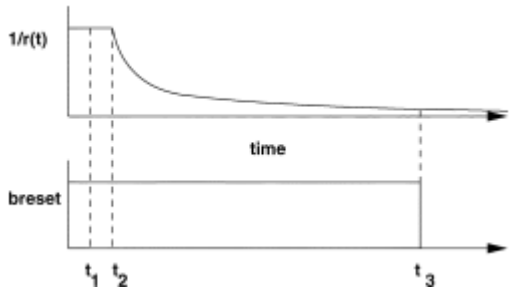

Figure 5.4: Bandwidth control timing waveforms

Hard reset is performed between t1 to t2 (shown in figure 5.4). At the end of hard reset, the noise voltage power across the sense node is $\frac{kT}{c_{se}+c_f}$. Between t2 and t3 the bandwidth of

M1 is reduced and eventually it approaches zero (when M1 is finally disconnected) thereby limiting the uncertainty in the Brownian motion of electrons associated with thermal noise.

M_{f1} serves dual purpose: it acts as a common source amplifier during the reset cycle and as a source follower during the readout process. During the reset operation, the photodiode capacitance c_{se} is controlled by M1 and common source transistor M_{f1} which acts as an error amplifier. During reset, switches breset and word are both closed. Before or after reset the voltage across c_{se} is read out when breset is open and word is closed. Now M_{f1} acts as a source follower. It has been reported that this technique minimizes the reset noise by 10 times (w.r.t. the hard reset noise) i.e. the reset noise power reduces to $\frac{kT}{10C}$.

5.3 Capacitive Control Method

The capacitive control technique reduces the reset noise without adding any image lag [42][40]. This circuit uses bandlimiting and capacitive feedback to reduce the reset noise.

The APS pixel of capacitive control method consists of two independent circuits – the reset circuit and the readout circuit. The readout circuitry is implemented using pixel level NMOS transistors M2 and M3 while the reset circuitry is implemented using pixel level NMOS transistors M1, M4, and M5 along with the column level operational amplifier as shown in figure 5.5 [42]. The circuit operation is as follows: firstly hard reset is performed by pulsing the signal V_{pr} high and bringing the photodiode voltage to ground. This eliminates image lag. Then the switch M5 is turned ON by pulsing the signal V_g high. The signal V_r rises slowly with a pre determined slope. As V_r is greater than V_{pd} the amplifier output is high and turns on the reset transistor M1. The photodiode now gets charged and it begins to follow the signal V_r. This occurs due to the intrinsic property of the op-amp that keeps its two inputs equal. Once V_r reaches its peak value, it drops by a few millivolts. This causes the photodiode voltage to

overshoot the signal V_r. The reason V_{pd} overshoots V_r instead of following V_r is because the transistor M1 can only act as a pull up transistor. Once V_{pd} exceeds V_r, the output of the amplifier goes low and turns OFF the reset transistor. The overlap capacitance of the transistor M1 controls V_{pd}. At the end of the reset period the signal V_g goes low and ends the reset operation. This is the basic operation of the capacitive control circuit and it uses the overlap capacitance to minimize the reset noise.

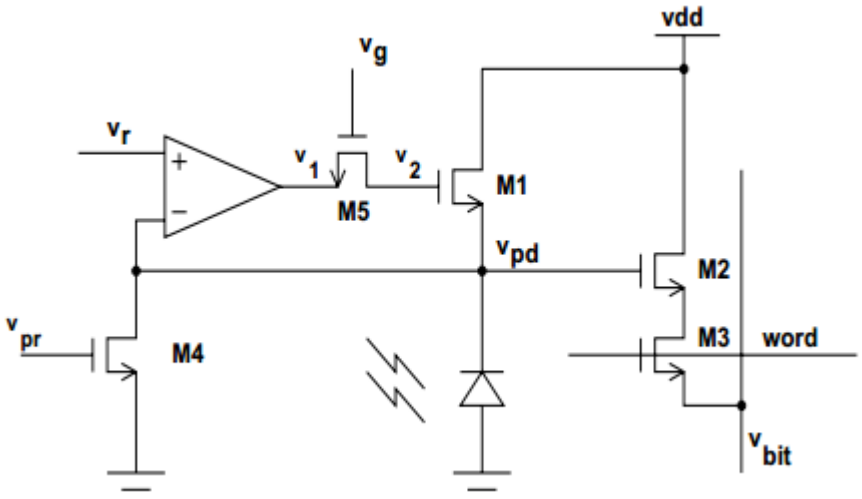

Figure 5.5: CMOS active pixel sensor with capacitive control technique

The unique feature about this method is that the circuit reaches steady state if the slope of the signal V_r rises slower than the feedback loop time constant. When the reset transistor M1 is turned OFF, reset noise is sampled into the photodiode. This noise power is the sum of the thermal noise from the reset amplifier and shot noise from M1. Shot noise from the photodiode and thermal noise from M5 being small is neglected. The relation between the input and output signals is shown in figure 5.6 [42].

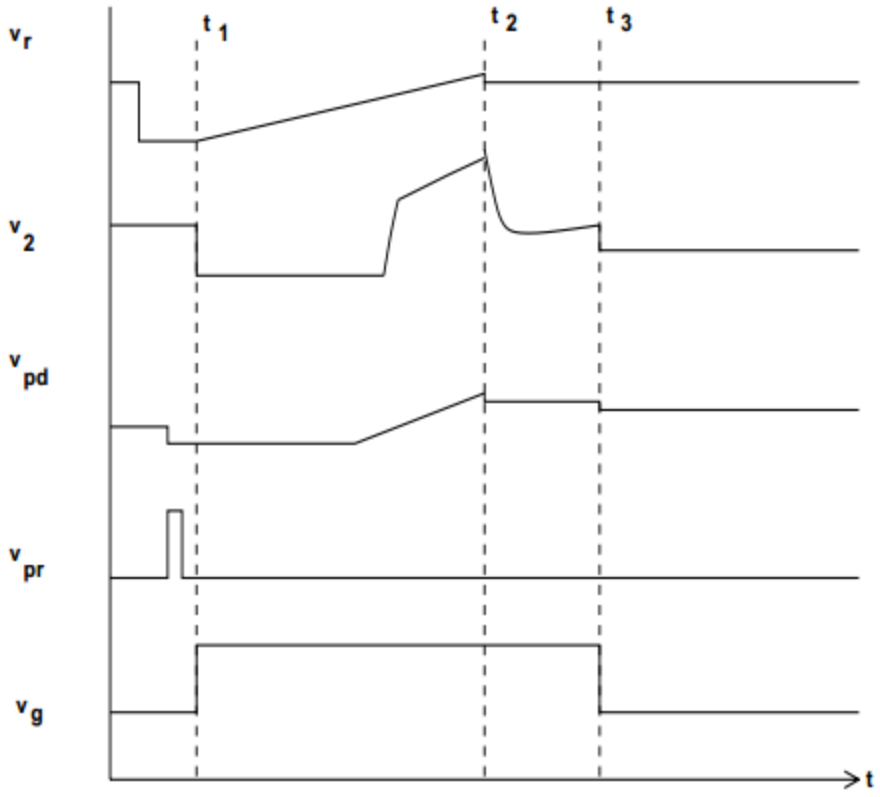

Figure 5.6: Input and output waveforms of the capacitive control circuit

This method uses a photodiode capacitance of 25.3 fF. For this value of capacitance the standard deviation from hard reset given by $\sqrt{\frac{kT}{C}}$ is 406 μV where T is 300K and k is $1.38\text{x}10^{-23}$ J/K. The measured standard deviation from capacitive control was reported to be 96 μV. The noise reduction is $\frac{406^2}{96^2} \cong 18$. This shows that the reset noise is reduced by a factor of 18 i.e. the output reset noise power is now reduced to $\frac{kT}{18C}$ as opposed to $\frac{kT}{C}$ for hard reset and $\frac{kT}{2C}$ for soft reset. Despite having a high reset noise reduction; this circuit uses 6 transistors per pixel resulting in very low fill factor.

5.4 Charge Control Method

The charge control technique reduces the reset noise by precisely determining when to stop charging the capacitive sensor after an initial hard reset [41][40]. This is another feedback technique to minimize the reset noise by comparing the pixel output voltage to a known reference voltage. The schematic of the circuit shown in figure 5.9 is a pixel level configuration with a column level comparator. This technique involves a three step process. First the photodiode is reset to V_{reset}, then a current source (M2) is connected to the photodiode to provide a discharge path for V_{se}, and once the output voltage V_n, falls below the reference value $V_{ref,}$ M2 is turned OFF, to bring the voltage across the photodiode to a known value, V_{ref}.

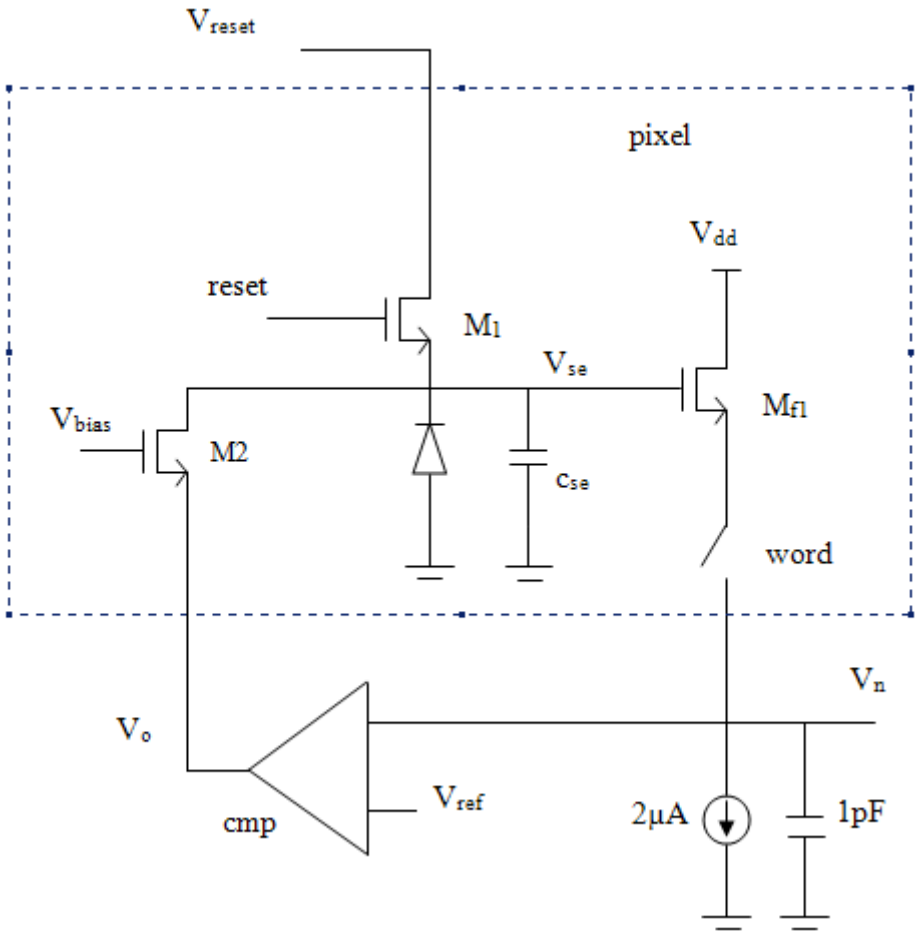

Figure 5.9: Schematic of the charge control technique

A hard reset is performed to flush out the residue charge from the previous exposure of the photodiode. It is then followed by soft reset operation in which both the signals reset and V_{reset} have the same voltage levels. The photodiode capacitance charges via M1 transistor which is turned on by the reset signal. Since the transistor operates in sub-threshold region (for soft reset) the photodiode voltage will not attain steady state with V_{reset}. After a few microseconds, the reset transistor is turned OFF abruptly. The timing for the input and output control signals for the charge control circuit is shown in figure 5.10.

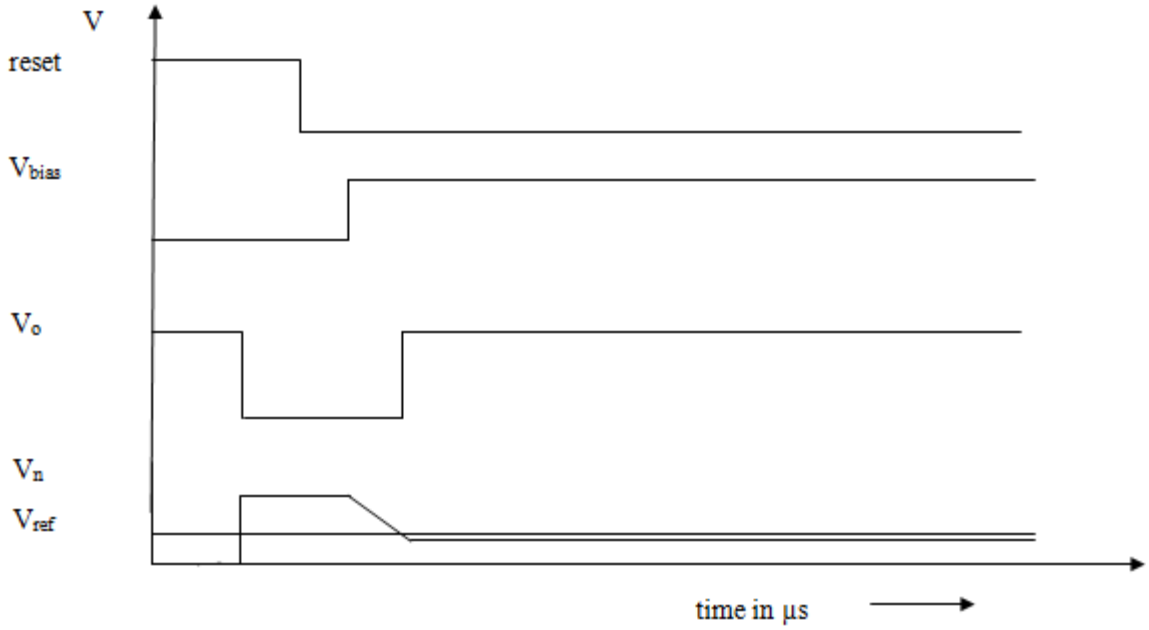

Figure 5.10: Input and output waveforms of charge control circuit

At this point reset noise is sampled into the photodiode. The pixel output voltage V_n, is read from the access transistor of the pixel when word signal goes high. This is connected to the negative terminal of a column level comparator. A fixed reference voltage V_{ref} is given to the positive terminal of the comparator. The reference voltage is selected to be less than the reset voltage of the pixel. As a result, the comparator outputs a low signal. A discharge path for the photodiode capacitance is created once the V_{bias} signal is applied (just a little over the threshold

voltage V_{th} to turn on the M2 transistor). The photodiode capacitor discharges along the path created by M2 and the output circuitry of the comparator (which is now low i.e. gnd). As the photodiode discharges, the pixel output voltage V_n, connected to the negative terminal of the comparator also decreases and at the point where it falls below the reference voltage V_{ref}, the comparator outputs a high signal. This instantly turns OFF the M2 transistor and freezes the voltage on the photodiode to be approximately equal to V_{ref}.

The accuracy of obtaining the reset voltage equal to the reference voltage and minimizing the reset noise depends upon the switching speed of the comparator and the magnitude of discharge current I_r. The input referred noise from the comparator is also considered in the noise analysis. Overall the noise voltage power on the photodiode is:

$$\sigma_{Vse}^2 = \sigma_{Vn1}^2 + \frac{qi_r\Delta t + i_r^2\sigma_{\Delta T}^2}{C_{se}^2} \tag{5.1}$$

Here σ_{Vn1}^2 is the variance of the input referred noise of the comparator and ΔT is the switching time of the comparator. Also $\Delta t = E[\Delta T]$ i.e. Δt is the expectation of the switching time of the comparator. In this paper, the following values are used to compute the noise reduction:

$\Delta t = 100$ ns, $\sigma_{\Delta T}^2 = 0$, $c_{se} = 6.7$ fF, $i_r = 0.23$ nA, $\sigma_{Vn1}^2 = 5.79$ nV^2, substituting these values: $\sigma_{Vse}^2 = 88$nV^2. The results from this paper show a reduction of 3.9 times in the reset noise i.e. $\frac{kT}{3.9C}$.

In this chapter some of the well known techniques for minimizing the reset noise were discussed including their design, circuit operation, and noise reduction mechanism. In the following chapter the new circuit proposed in this documentation is presented.

CHAPTER SIX: NEW CIRCUIT PROPOSED FOR RESET NOISE REDUCTION

6.1 Introduction

As discussed in the previous chapters, reset noise plays a significant role in limiting the detection of the photodiode based CMOS image sensor, especially in low light conditions. In a standard active pixel sensor (APS) the reset noise (i.e. the hard reset noise) is of the order of $\frac{kT}{C}$. This noise basically results from the random fluctuations in the charge (or voltage) on the photodiode due to intrinsic noise in the reset FET (field effect transistor). These random fluctuations are frozen on the photodiode capacitance when the pixel is disconnected from the reset FET. Therefore reset noise can be suppressed by reducing the amount of random fluctuations during reset.

Some of the published methods for reducing the reset noise were discussed in chapter five of this documentation. In this chapter, a new circuit of the CMOS image sensor with significant reduction in the reset noise using the charge control technique is presented. In this technique, the reset noise is reduced by precisely determining when to stop charging the capacitive sensor using feedback. The voltage across the photodiode is monitored by employing a column level comparator which is part of a feedback circuit connected directly to the reset transistor. Also in this new circuit, the idea of using a ramp signal V_{reset} instead of a dc signal to charge the sense node (photodiode capacitance) is presented. The reduced noise is a result of precisely controlling the slope of the ramp signal $V_{reset.}$ The slope of V_{reset} is changed slower than the time constant of the feedback circuit. This ensures that the feedback is faster than the rate at which noise is added to the sense node**.**

6.2 System level and pixel level overview of the proposed circuit

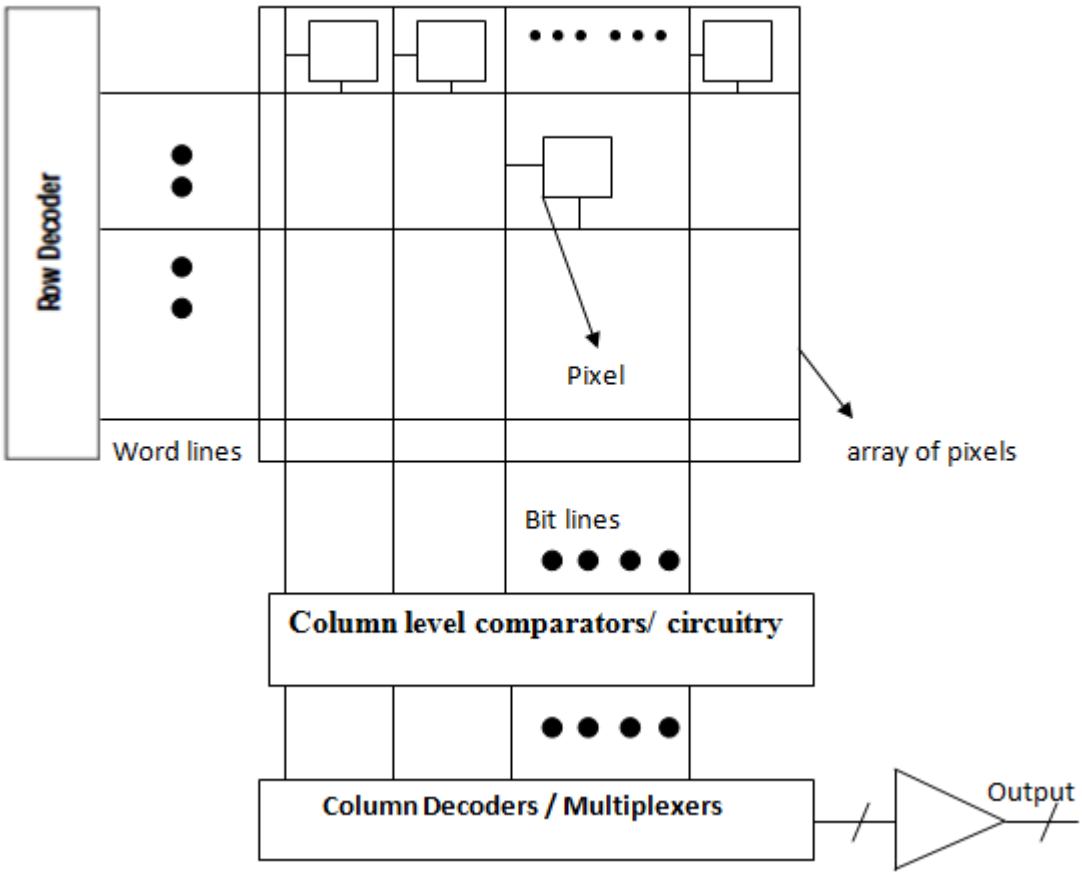

Figure 6.1: System level block diagram

The image sensor consists of an array of pixels. All the pixels in a column share the same column level circuitry. So, at a time only one pixel from a column is selected. The pixels are selected one row at a time using the row decoder. A row of pixels is selected when its Word line goes high. All the Bit lines go high at the same time to connect the pixels of the selected row to their corresponding column level circuit. Readout is done by transferring one row at a time to column storage capacitors and then its read out using column decoders and multiplexers. This is the typical operation of any standard CMOS image sensor. The system level block diagram is shown in figure 6.1. The new circuit proposed in this chapter is the design for each individual pixel of the array. Each pixel has a photodiode and four transistors for reset and readout.

6.3 Circuit Operation

The circuit shown in figure 6.2 is the pixel level schematic of the new circuit. This circuit uses the charge control technique to minimize the reset noise. It monitors the photodiode voltage, V_{se} using a column level comparator, cmp. This column level comparator directly controls the operation of the reset transistor M1 through Col_switch. Also a ramp signal V_{reset} instead of V_{dd} is used to precisely control the rate at which the photodiode capacitance c_{se}, charges. This technique is compatible with implementing the two dimensional imaging array for the sensor.

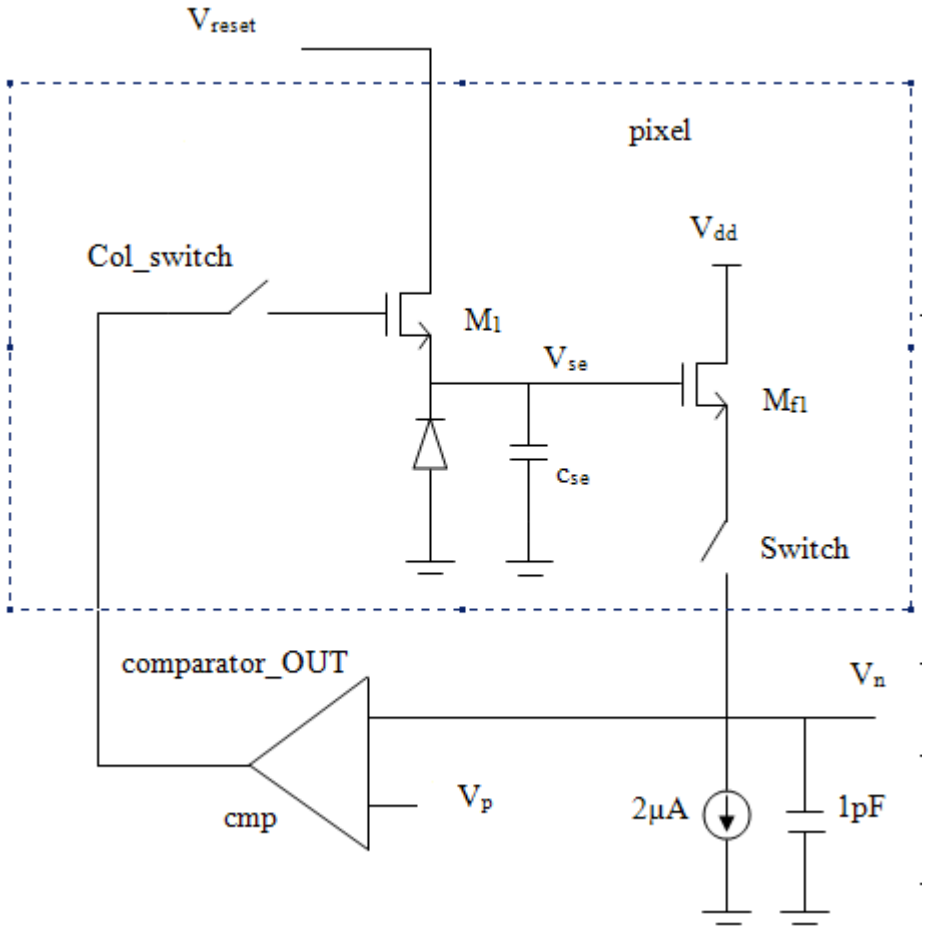

Figure 6.2: Schematic for the new circuit

To begin with, the array of pixels in the imager is reset. Reset operation is performed row wise i.e. one row of pixels is reset at a time. Every pixel in the selected row has a corresponding

column level circuitry to aid the reset process. A pre-determined fixed dc voltage V_p, used as reference, is connected to the positive terminal of each column level comparator. The output voltage V_n read out of the selected pixel is connected to the negative terminal of the comparator. The output from the comparator controls the gate of the reset transistor M1, through Col_switch, as shown in figure 6.2. To start with the pixel voltage V_n, is lesser than V_p (from the previous exposure), so the comparator sends out a high signal as output. This turns on the reset transistor M1. Now the V_{reset} signal is connected to the photodiode through M1. V_{reset} is set to 0V for the first µs of the reset operation. This flushes out any residue charge remaining in the photodiode from the previous exposure. Then the V_{reset} signal rises slowly with an optimum slope (the slope must be smaller than the feedback loop time constant) to charge the photodiode.

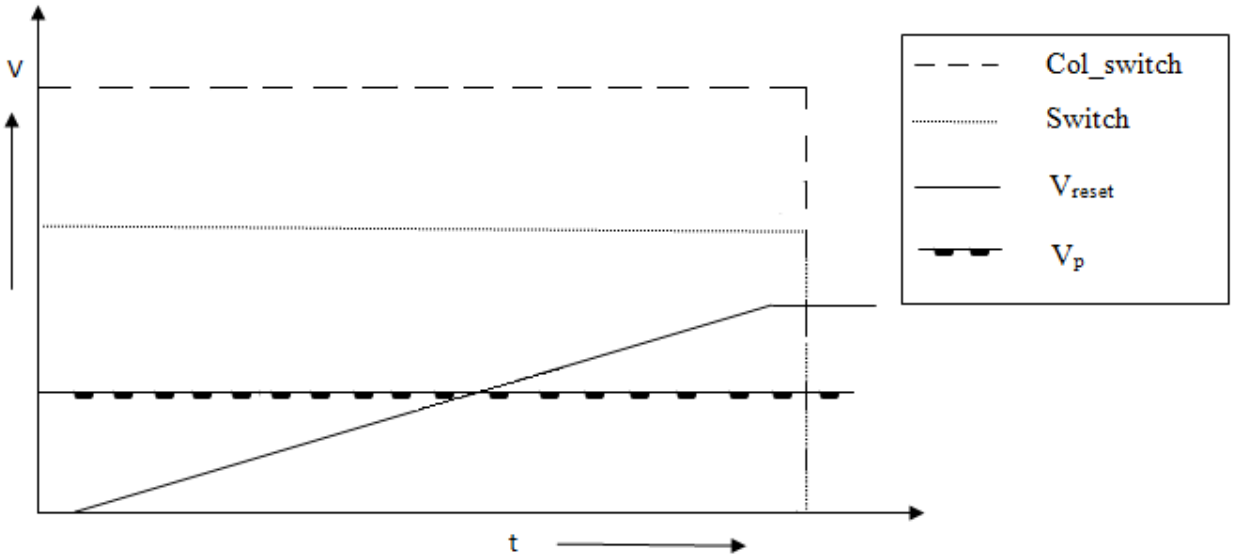

Figure 6.3: Timing diagram for the input signals

The input timing control signals are shown in figure 6.3. There is a drop equal to the threshold voltage across the source follower M_{f1}. The pixel output voltage V_n, is read out of the pixel by pulsing the word signal high. This is connected to the column level comparator and compared with V_p. As soon as V_n exceeds V_p, the comparator outputs a low signal and instantly

turns OFF the reset transistor M1. The slope of the ramp signal V_{reset} is chosen such that it changes slower than the feedback loop time constant. This way the feedback precisely controls when to stop charging the photodiode and reduces the reset noise significantly. The signals Col_switch and switch are set to low at the end of the reset operation to deselect the pixel. The output timing is shown in figure 6.4.

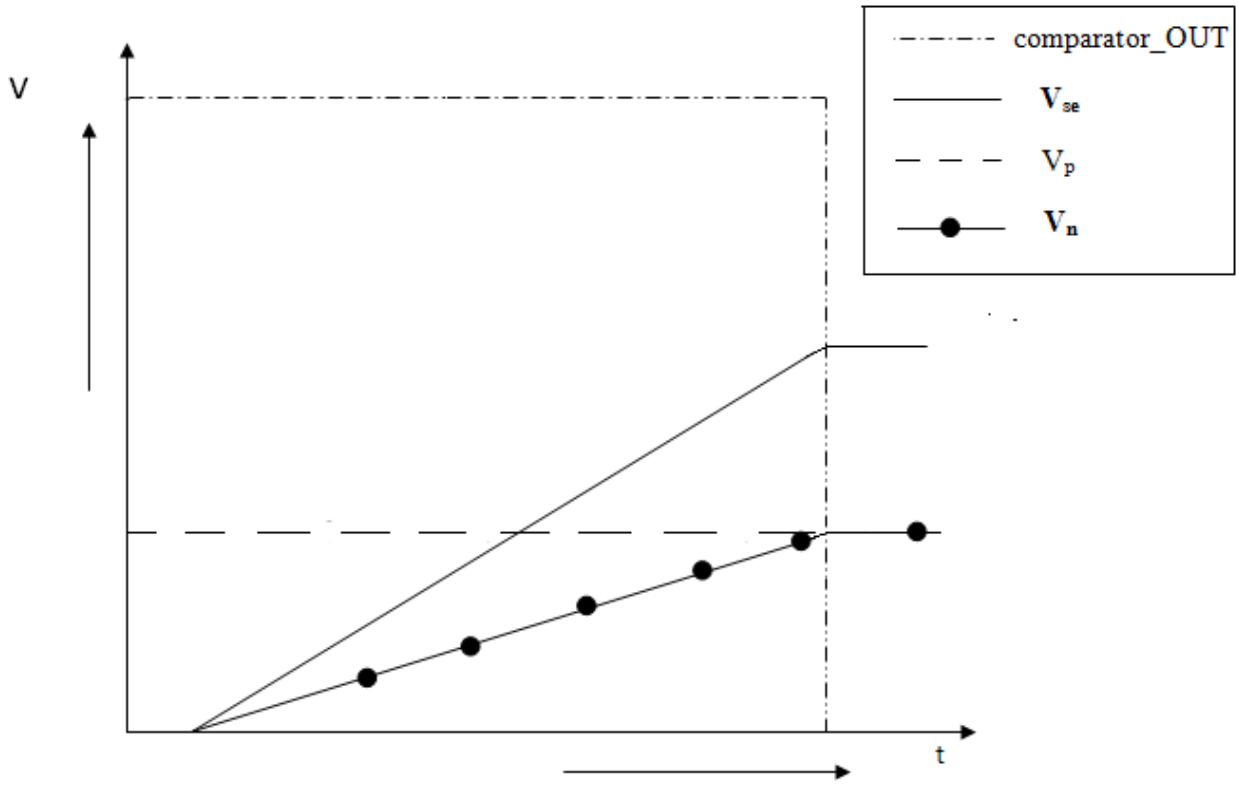

Figure 6.4: Timing diagram for the output signals

Here the reset transistor M1, acts as a switch i.e. it operates in the linear region. The photodiode voltage V_{se}, follows V_{reset} and the later is constantly increasing at a pre-determined slope. So the voltage at the drain of M1 is always higher than its source. This ensures a unidirectional flow of current between the photodiode and drain of M1. In other words, thermal equilibrium is not reached. As discussed in the previous chapters, this is a mandatory requirement to optimally control the reset noise. Even though the reset transistor is operated in

the linear region, the use of ramp signal in the drain supply (V_{reset}) instead of a dc voltage allows this new circuit to have soft reset. Also this technique does not introduce any additional lag as soft reset is preceded by hard reset. It is possible to precisely control the rate of current charging the photodiode by varying the slope of $V_{reset.}$ This is one of the major advantages over the conventional charge control technique where the rate of discharge of the photodiode current cannot be controlled.

6.3.1 Column level comparator

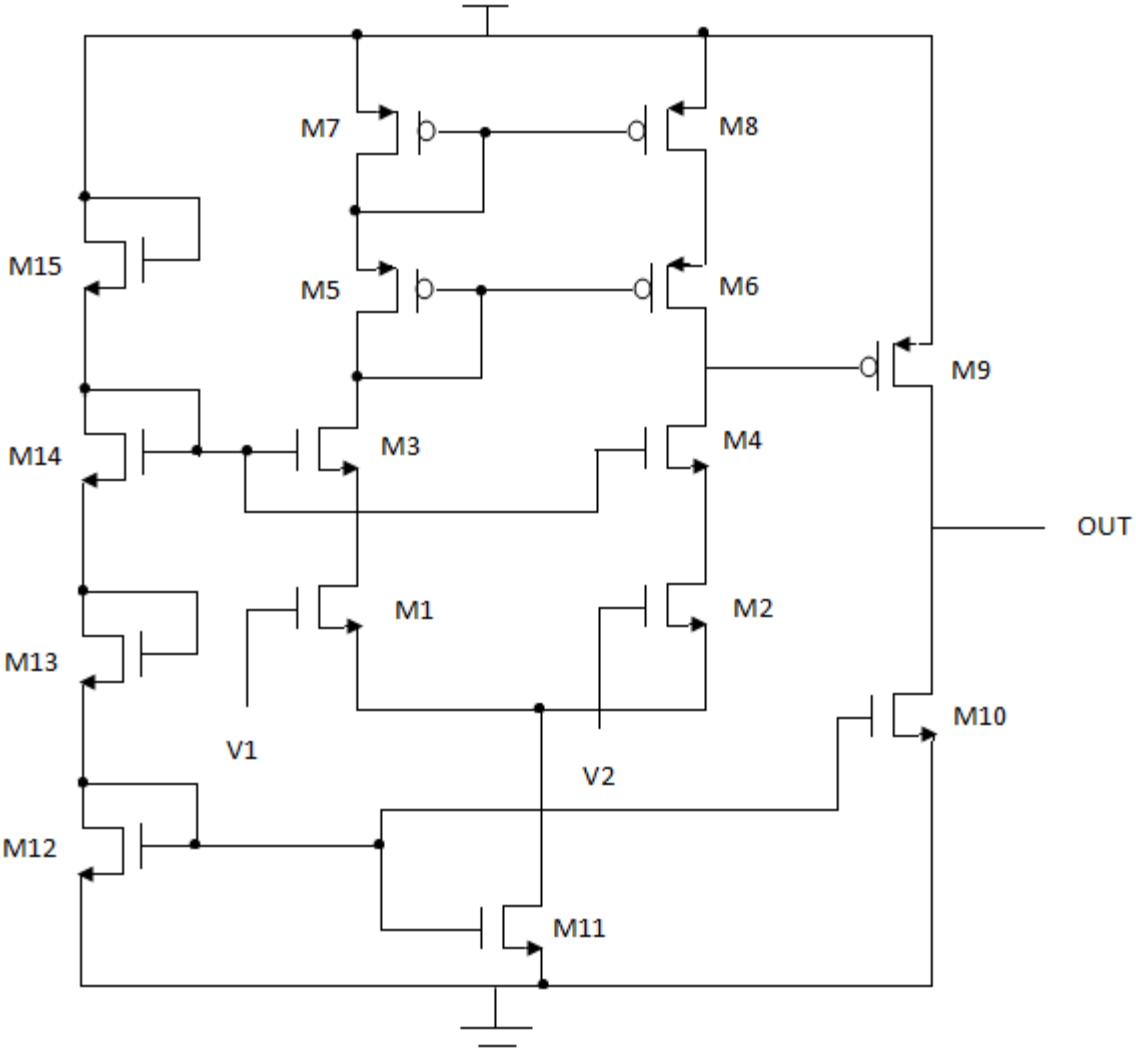

Figure 6.5: Column level comparator circuit

In the figure 6.5 the schematic of the column level comparator used in the testing of this new circuit is shown. This comparator is a high gain operational amplifier designed using two stages. The first stage is an active load differential amplifier while the second stage is common source stage. The two stages give a combined gain of 95dB. The input signals to be compared i.e. the pixel output voltage V_n, and the reference voltage V_p, are given to the input terminals V1 and V2 shown in the figure 6.5. The circuit compares the input signals and depending on the result of the comparison, OUT gives a high or low signal. If V2 is higher than V1 then OUT is high, else OUT is low. Table 6.1 shows the component values of the transistors used.

Table 6.1: Column level comparator simulation component parameters

Component	Parameter	Value	Units
M1, M2	$\frac{W}{L}$	$\frac{84}{1.8}$	µm
M3, M4	$\frac{W}{L}$	$\frac{1.2}{2.4}$	µm
M5, M6	$\frac{W}{L}$	$\frac{2.4}{3.0}$	µm
M7, M8	$\frac{W}{L}$	$\frac{1.8}{0.6}$	µm
M9	$\frac{W}{L}$	$\frac{1.8}{0.6}$	µm
M10	$\frac{W}{L}$	$\frac{6.6}{1.2}$	µm
M11	$\frac{W}{L}$	$\frac{1.8}{12}$	µm

M12, M13, M14, and M15 are used for biasing and are part of a current mirror circuit.

6.4 Noise Analysis for the new circuit

The noise power of the voltage across the photodiode for the new circuit is derived in this section. The total noise power is the summation of noise contributed by thermal noise from M1, shot noise from the photodiode, and the input referred noise from the comparator. Let T_{sw} be the time at which the column level comparator switches from high to low, ΔT be the switching time of the comparator, c_{se} be the photodiode capacitance, and $I_d(\tau)$ be the current charging the photodiode in the pixel. The voltage across the photodiode is:

$$V_{se} = V_{se}(0) + \frac{1}{c_{se}} \int_0^{T_{sw}+\Delta T} I_d(\tau)\, d\tau \tag{6.1}$$

$V_{se}(0)$, T_{sw}, and ΔT are random variables. Here $T_{sw} + \Delta T$ are the total time for which the reset transistor M1 is ON. Hence it allows the charging of the photodiode capacitance during this period. At time 0 the voltage on the photodiode is 0V. This is because the signal V_{reset} is set to 0V for a period of 1µs to remove image lag. Hence $V_{se}(0)$ is 0V. Equation (6.1) can be re-written as:

$$V_{se} = V_{se}(T_{sw}) + \frac{1}{c_{se}} \int_{T_{sw}}^{T_{sw}+\Delta T} I_d(\tau)\, d\tau \tag{6.2}$$

We know that $\int_0^t \frac{I_d(\tau)}{q} d\tau$ is a Poisson process with parameter $\frac{i_d}{q}$ [10]. Also

$$E\left[\int_0^t \frac{I_d(\tau)}{q} d\tau\right] = \frac{i_d t}{q} \tag{6.3}$$

Equation (6.2) can be re-written as:

$$V_{se} = V_{se}(T_{sw}) + \frac{q}{c_{se}} \int_0^{\Delta T} \frac{I_d(\tau)}{q} d\tau \tag{6.4}$$

Let $\Delta t = E[\Delta T]$ and $\sigma_{\Delta T}^2 = E[(\Delta T - \Delta t)^2]$

Let $E[V_{se}]$ be the expected voltage across the capacitive sensor after reset.

$$E[V_{se}] = E[V_{se}(T_{sw})] + E[\frac{q}{c_{se}} \int_0^{\Delta T} \frac{I_d(\tau)}{q} d\tau \quad (6.5)$$

Using the equation $E[g(X,Y)] = E[E[g(X,Y)|Y]]$, (6.5) can be re-written as:

$$E[V_{se}] = E[V_p+V_{n1}] + E[E[\frac{q}{c_{se}} \int_0^{\Delta T} \frac{I_d(\tau)}{q} d\tau \mid \Delta T]] \quad (6.6)$$

The assumption is that $V_{n1}(t)$ is a white random process with zero mean and variance as σ_{Vn1}^2.

$$E[V_{se}] = V_p + E[\frac{I_d \Delta T}{c_{se}}] \quad (6.7)$$

$$E[V_{se}] = V_p + \frac{I_d \Delta t}{c_{se}} \quad (6.8)$$

The noise power across the photodiode from the new proposed circuit is the expectation of the square of the difference between the voltage across the capacitive sensor when the comparator switches to turn OFF the reset transistor M1 and the expected value of voltage across the capacitive sensor at the end of the reset.

$$\sigma_{Vse\_comp}^2 = E[(V_{se}(T_{sw}) + \frac{q}{c_{se}} \int_0^{\Delta T} \frac{I_d(\tau)}{q} d\tau - V_p - \frac{I_d \Delta t}{c_{se}})^2] \quad (6.9)$$

Here $V_{se}(T_{sw})$ and $\int_0^{\Delta T} \frac{I_d(\tau)}{q} d\tau$ are uncorrelated. So (6.9) can be re-written as:

$$= E[(V_{se}(T_{sw}) - V_p)^2] + E[(\frac{q}{c_{se}} \int_0^{\Delta T} \frac{I_d(\tau)}{q} d\tau - \frac{I_d \Delta t}{c_{se}})^2] \quad (6.10)$$

$$= \sigma_{Vn1}^2 + E[E[(\frac{q}{c_{se}} \int_0^{\Delta T} \frac{I_d(\tau)}{q} d\tau - \frac{I_d \Delta t}{c_{se}})^2 \mid \Delta T]] \quad (6.11)$$

$$= \sigma_{Vn1}^2 + E[\frac{1}{c_{se}^2}(q i_d \Delta T + i_d^2 \Delta T^2) - \frac{2 i_d^2 \Delta t \Delta T}{c_{se}^2} + \frac{i_d^2 \Delta t^2}{c_{se}^2}] \quad (6.12)$$

$$= \sigma_{Vn1}^2 + \frac{qi_d\Delta t + i_d^2(\sigma_{\Delta T}^2 + \Delta t^2)}{c_{se}^2} - \frac{2i_d^2\Delta t^2}{c_{se}^2} + \frac{i_d^2\Delta t^2}{c_{se}^2} \quad (6.13)$$

$$= \sigma_{Vn1}^2 + \frac{qi_d\Delta t + i_d^2\sigma_{\Delta T}^2}{c_{se}^2} \quad (6.14)$$

Since $\sigma_{\Delta T}^2$ is negligibly small the term $i_d^2\sigma_{\Delta T}^2$ can be ignored.

$$\sigma_{Vse\_comp}^2 = \sigma_{Vn1}^2 + \frac{qi_d\Delta t}{c_{se}^2} \quad (6.15)$$

The reset transistor M1 is operating in the linear region. The thermal noise added by M1 is given by:

$$\sigma_{Vse\_thermal}^2 = \int_{-\infty}^{+\infty} PSD\,|H(f)|^2\,df \quad (6.16)$$

Here PSD is the power spectral density and for transistor operating in linear region it is given by:

$$PSD = 2kTR \quad (6.17)$$

$$PSD = \frac{2kT}{k_n' \frac{W}{L}(V_{gs} - V_{th})} \quad (6.18)$$

W = 1.5µm, L = 0.6µm, $k_n' = 1.32\text{x}10^{-4}$ A/V^2, $k = 1.38\text{x}10^{-23}$ J/K, T = 300K, β is the gain of the feedback circuit which is of the order of 95dB, A is the gain from the pixel, hence the product βA >> 1. So the transfer function is:

$$|H(f)|^2 = \left|\frac{1}{\beta}\left(1 - \frac{1}{\beta A}\right)\right|^2 \quad (6.19)$$

Substituting the above values the term $\sigma_{Vse\_thermal}^2$ is of the order of $2.28\text{x}10^{-17}$ V^2. The total reset noise power across the photodiode at the end of the reset operation is:

$$\sigma_{Vse}^2 = \sigma_{Vse\_thermal}^2 + \sigma_{Vse\_comp}^2 \quad (6.20)$$

Substituting the expressions derived for $\sigma_{Vse\_thermal}^2$ and $\sigma_{Vse\_comp}^2$, the final expression is approximated to:

$$\sigma_{Vse}^2 = \sigma_{Vn1}^2 + \frac{qi_d\Delta t}{c_{se}^2} \tag{6.21}$$

Here Δt is the switching time of the comparator and is of the order of 100 ns, q is the charge of an electron and is equal to 1.602×10^{-19} Coulombs, i_d is the current through the pixel i.e. it is the rate at which the photodiode capacitance gets charged. As discussed earlier, it is possible to control the current in the pixel by modifying the slope of the V_{reset} signal. For this derivation i_d value of 0.25nA is used. Also the photodiode capacitance c_{se} is equal to 25fF. Substituting these values into the equation, the derivation of the final reset noise power from the proposed circuit is given by:

$$\sigma_{Vse}^2 = \sigma_{Vn1}^2 + \frac{qi_d\Delta t}{c_{se}^2} \tag{6.22}$$

$$= 2\text{x}10^{-9} + \frac{1.602x10^{-19} * 0.25x10^{-9} * 100x10^{-9}}{(25x10^{-15})^2} \tag{6.23}$$

$$= 8.408\text{x}10^{-9}\ \text{V}^2 \tag{6.24}$$

Also $q_{se} = V_{se}c_{se}$, so

$$\sigma_{qse}^2 = \sigma_{Vse}^2 c_{se}^2 \tag{6.25}$$

Substituting from (6.21) the input referred charge noise on the photodiode is given by:

$$\sigma_{qse}^2 = c_{se}^2\sigma_{Vn1}^2 + qi_d\Delta t \tag{6.26}$$

6.5 Simulation Results

The simulation for this proposed circuit was done using 0.5µm CMOS process with cadence virtuoso tool. The transient noise analysis results were obtained with BSIM3 level 3 SPICE model. All the in-pixel transistors are minimum size transistors. The column level

comparator has a high gain of 95 dB. For this simulation the slope of V_{reset} signal is set to 0.1345 V/µs, power supply V_{dd} is 5V, photodiode capacitance c_{se} is 25fF. The other input and the output signals are shown in figure 6.6 and figure 6.7 respectively.

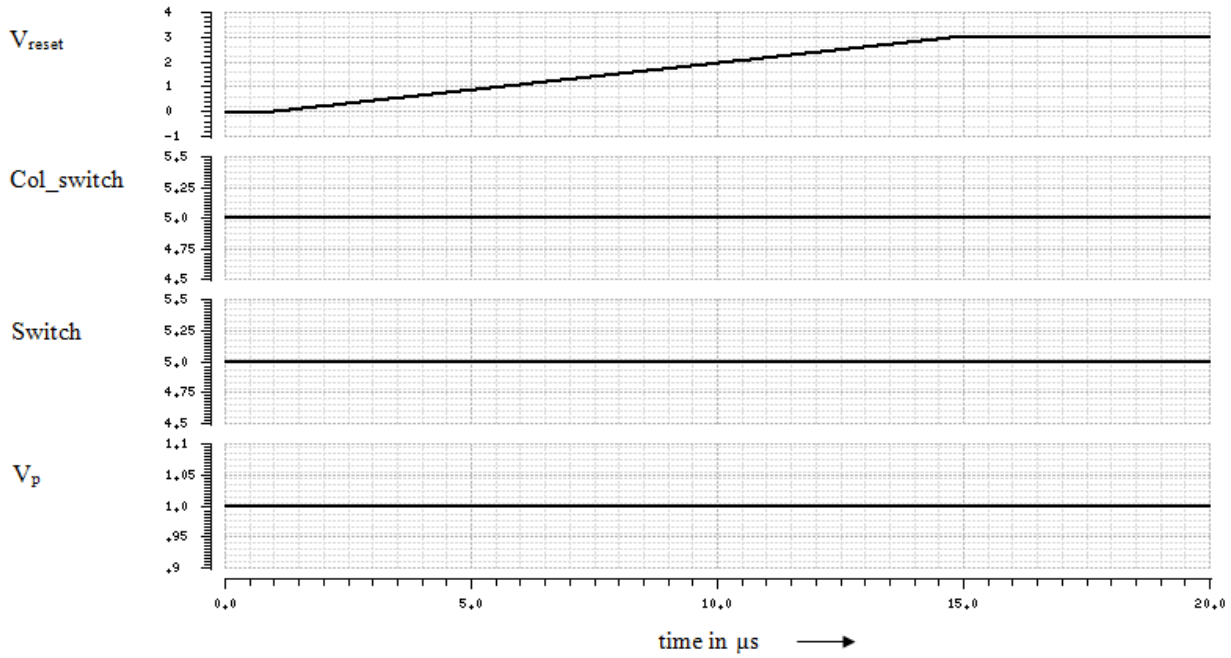

Figure 6.6: Input signal waveforms for the new circuit

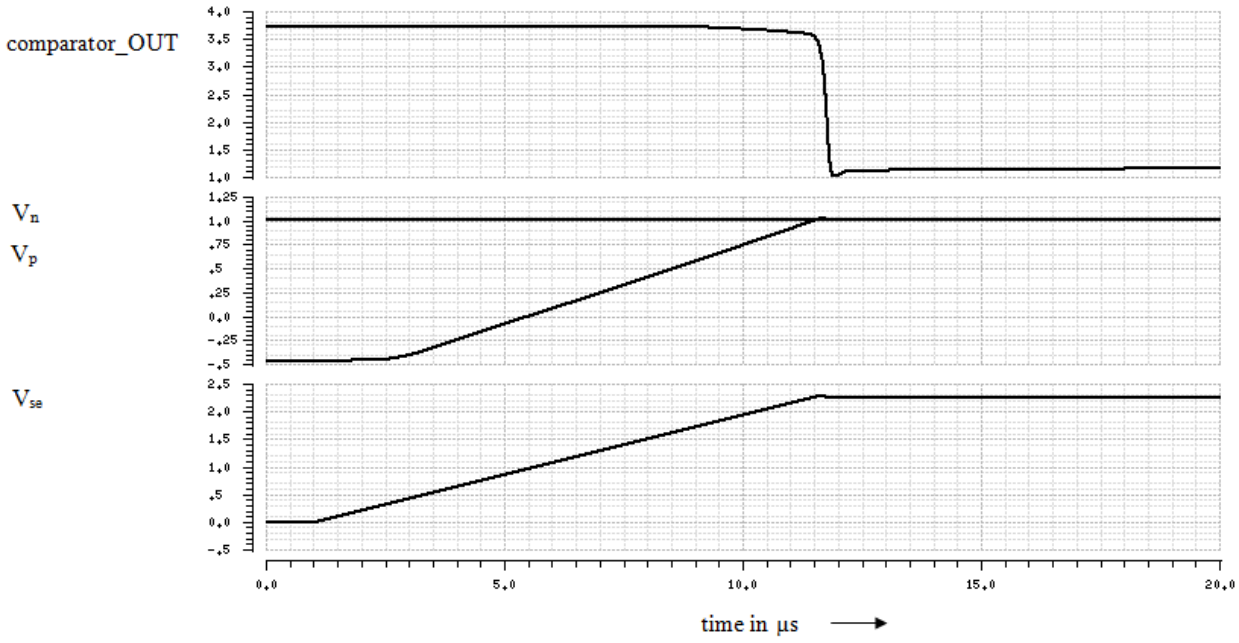

Figure 6.7: Simulation results of the output signals using transient noise analysis

The input signals Col_switch and Switch are used for pixel selection. The output signal V_{se} follows the input signal $V_{reset.}$ When the pixel output voltage V_n, equals the reference voltage V_p, the comparator_OUT switches to a low signal and turns OFF the reset transistor, M1. The photodiode is now reset to a voltage equal to the reference voltage V_p which is 1.1 V in the above simulation.

A Monte Carlo simulation of the transient noise analysis was done with 128 iterations. All the iterations were run with F_{max} = 1GHz, temperature T = 300K, photodiode capacitance c_{se} = 25fF, and I_{se} = 2.53pA. The transient noise waveforms shown below plot the standard deviation and variance of the transient noise as a function of time. As discussed before this technique allows to precisely control the reset noise added to the photodiode capacitance by adjusting the slope of the V_{reset} signal. As the slope varies the duration of reset also changes. For a slower slope, the reset period increases but the noise power decreases. For a faster slope the reset period is small but the noise added is higher. So there is a tradeoff between speed and reset noise. These waveforms are plotted for three different values of slope of the V_{reset} signal:

Case 1: Slope of V_{reset} signal as $\frac{3}{15}$ = 0.2 V/µs

Case 2: Slope of V_{reset} signal as $\frac{3}{21}$ = 0.1428 V/µs

Case 3: Slope of V_{reset} signal as $\frac{3}{28}$ = 0.107 V/µs

In all the three cases, the V_{reset} was increased from 0V to 3V. The signal was held at 0V for the first µs of the reset operation to flush the residue charge from c_{se}. For each value of slope the response of the standard deviation σ_{Vse} of transient noise is followed by the plot of the noise power σ_{Vse}^2 as a function of time.

Case 1: Noise Response for slope of V_{reset} signal as 0.2 V/µs

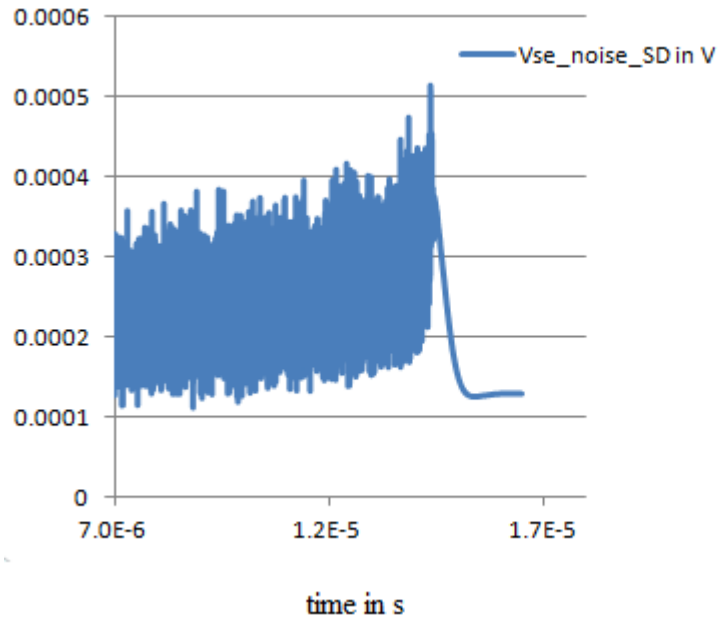

Figure 6.8: Case 1: Transient noise waveform of σ_{Vse} vs. time

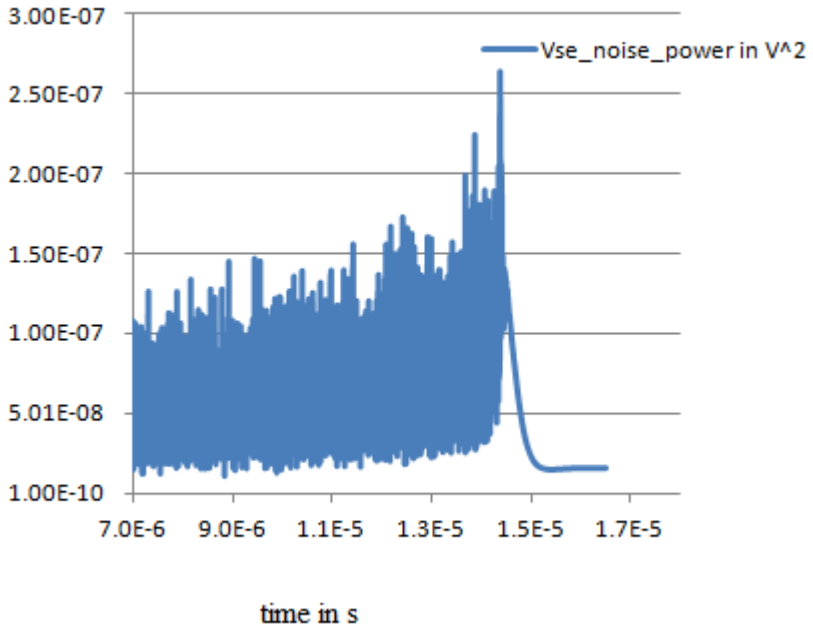

Figure 6.9: Case 1: Transient noise waveform of σ_{Vse}^2 vs. time

Case 2: Noise Response for slope of V_{reset} signal as 0.1428 V/µs

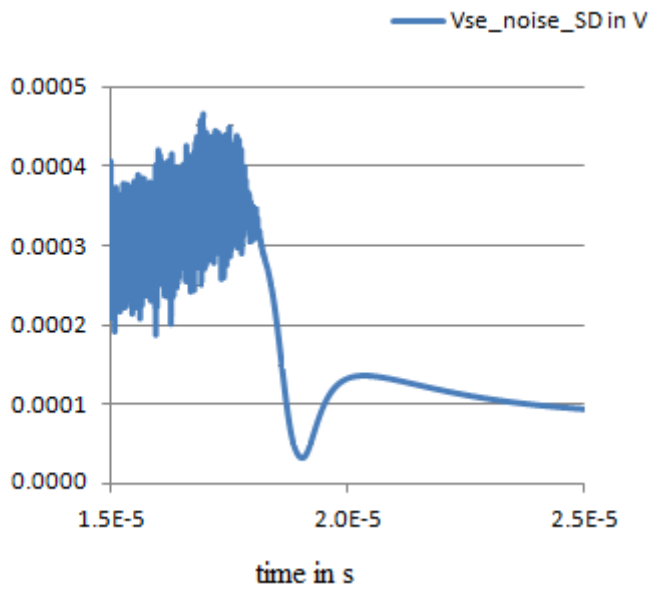

Figure 6.10: Case 2: Transient noise waveform of σ_{Vse} vs. time

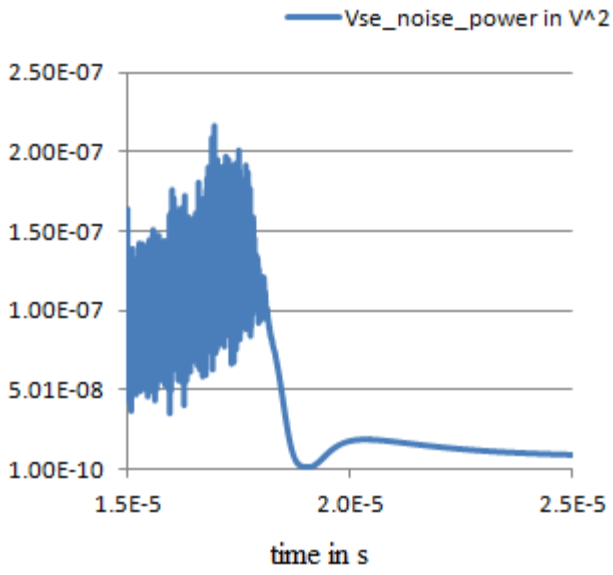

Figure 6.11: Case 2: Transient noise waveform of σ_{Vse}^2 vs. time

Case 3: Noise Response for slope of V_{reset} signal as 0.107 V/µs

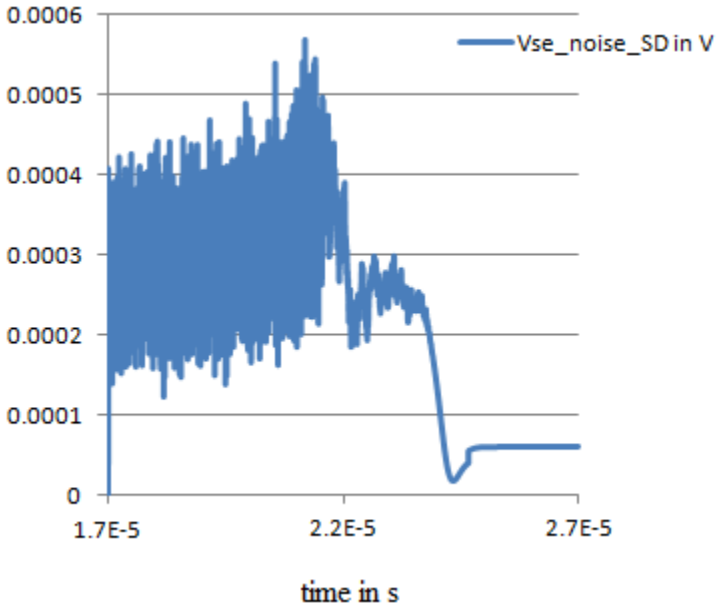

Figure 6.12: Case 3: Transient noise waveform of σ_{Vse} vs. time

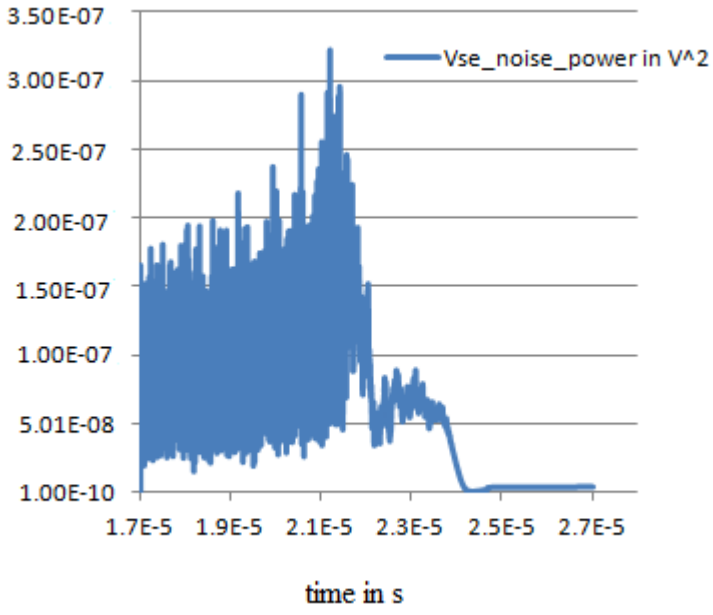

Figure 6.13: Case 3: Transient noise waveform of σ_{Vse}^2 vs. time

On comparing the transient noise waveforms shown above, there is a pattern observed between the noise response and the slope of the V_{reset} signal. As the slope of V_{reset} is decreased

the reset noise power also decreases. This is because when the slope of V_{reset} is small the rate of noise addition to the sense node during the switching of the comparator is lesser compared to the case when the slope of V_{reset} is higher. Using a column level comparator with a high switching speed and V_{reset} with slope slower than the time constant of the feedback it is possible to precisely minimize the reset noise.

In this section the reduction in reset noise power is computed using the simulation results obtained from case 3 i.e. with slope = 0.107 V/µs. The noise variance from hard reset is given by $\frac{kT}{c_{se}}$. Substituting for k = 1.3806503×10^{-23} J/K, T = 300 K, and c_{se} = 25 fF:

$$\text{Noise variance by hard reset, } \sigma_{hardreset}^2 = \frac{kT}{c_{se}} \quad (6.27)$$

$$= 1.65678036 \times 10^{-7}\ V^2 \quad (6.28)$$

$$\text{Standard deviation by hard reset, } \sigma_{hardreset} = \sqrt{1.65678036 \times 10^{-7}} \quad (6.29)$$

$$= 407.036\ \mu V \quad (6.30)$$

The standard deviation of the photodiode voltage σ_{Vse} at the end of reset operation is 85µV (refer figure 6.10). Thus the RNRF (Reduced Noise Reduction Factor) from the new circuit is given by:

$$RNRF = \left(\frac{\sigma_{hardreset}}{\sigma_{Vse}}\right)^2 \quad (6.31)$$

$$= \left(\frac{407.036}{85}\right)^2 \quad (6.32)$$

$$= (4.788)^2 \quad (6.33)$$

$$= 23 \quad (6.34)$$

This implies that the reset noise power can be reduced to $\frac{kT}{23C}$ and more with this new circuit proposed. Using the expression for input referred charge noise from (6.26) we can compute the $\frac{\sigma_{qse}}{q}$ term.

Table 6.2: Comparison of simulation results – reset noise power and slope of V_{reset}

Slope Of V_{reset} in V/µs	**Reset Standard Deviation, σ_{Vse} in µV**	**Reset Noise Power, σ_{Vse}^2 in μV^2**	**Noise Reduction**	**RNRF**	**$\frac{\sigma_{qse}}{q}$ in e-rms**
0.2	119	1.416×10^{-8}	$\frac{kT}{12c}$	12	22.5
0.1428	94	8.836×10^{-9}	$\frac{kT}{19c}$	19	15
0.107	78	6.084×10^{-9}	$\frac{kT}{23c}$	23	13.5

The simulation results in Table 6.2 are obtained from the transient noise waveforms of standard deviation σ_{Vse} and noise variance σ_{Vse}^2 of the photodiode voltage V_{se} shown in figures 6.8- 6.13. The RNRF for each slope of V_{reset} is computed as the ratio of σ_{Vse} of the photodiode in hard reset to σ_{Vse} of the photodiode using the new circuit. A sample of this calculation is shown in equation (6.30) and (6.34). These results show that by controlling the slope of the V_{reset} signal, it is possible to control the rate at which the photodiode gets charged and thereby reduce the reset noise significantly.

Table 6.3 summarizes the properties of the new circuit proposed in this chapter.

Table 6.3: Circuit parameters and results of transient noise analysis of the new circuit

Parameter	Units	Value
Reduced noise reduction factor (RNRF)		≥ 23
Technology	µm	0.5
Additional Image Lag		None
Swing	V	1.25
V_{dd}	V	5

CONCLUSION

In this thesis, the operation of image sensors used in digital cameras is discussed. The design, behavior, and noise in CMOS image sensors were analyzed in detail. In the noise analysis, it was established that reducing the reset noise would improve the sensitivity of the image sensor to a great extent. Some of the existing circuits for reducing the reset noise were discussed.

Also a new pixel level circuit using the charge control mechanism was proposed. In this circuit a linear ramp signal V_{reset} is used to charge the photodiode sensor instead of the conventional dc voltage supply. Also the column level feedback directly controls the reset switch in the pixel. The noise analysis and the simulation results of this circuit show reset noise reduction of the order of $\frac{kT}{23C}$ or more. Monte Carlo simulation of the transient noise analysis was performed for three different scenarios (obtained by modifying the slope of the input V_{reset} signal) and the results were tabulated. The simulation results show a decrease in the reset noise power with increase in the reset duration. When the slope of V_{reset} is reduced the rate at which the photodiode sensor gets charged is also reduced. So the feedback becomes faster than the rate at which noise is added to the photodiode capacitive sensor reducing the reset noise significantly.

The Table 7 compares the performance of some of the most commonly known techniques employed for reset noise reduction in CMOS image sensors. The comparison is based on several parameters like Reduced Noise Reduction Factor (RNRF), number of transistors (T) per pixel, technology used, voltage swing, and the supply voltage used.

Table 7: Summary of noise performance

Method	RNRF	# of T per pixel	Tech (µm)	Swing (V)	V_{dd} (V)
Bandwidth Control (BC) [39]	14	3	0.25	0.8	3.3
Capacitive Control [42]	18	6	0.35	1	3.3
Charge Control (CHC) [41]	3.9	4	0.18	0.4	1.8
BC & CHC [32]	10	4	0.5	0.975	5.0
New circuit	23	4	0.5	1.25	5.0

On comparing the results in Table 7, we may conclude that the new circuit presented has a high reset noise reduction factor and also meets the other specifications such as high fill factor, and acceptable levels of voltage swing with no additional image lag.

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VITA

Nitya Syamsundar was born and raised in India. She obtained her Bachelors degree in Electronics and Communication Engineering from Anna University, India in 2007. Then she gained some industry experience for 2 years. She proceeded to do her Masters in Electrical Engineering from the University of Texas at San Antonio, USA in 2011. After her master's degree she will pursue a career in the hardware industry.